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New Optimal Pulsewidth Modulation for Single DC-Link Dual Inverter fed Open-end Stator Winding Induction Motor Drive

Amarendra Edpuganti, *Student Member, IEEE* and Akshay K. Rathore, *Senior Member, IEEE*

***Abstract*—The multilevel topology with dual inverters feeding both ends of an open-end stator winding of an induction motor has been introduced around two decades ago. A common-mode inductor is usually required in series with motor windings to suppress zero-sequence or common-mode currents. In case of medium voltage high power drives, low device switching frequency operation is preferred to improve the overall system efficiency. However, it increases the harmonic distortion of machine stator currents. Therefore, the goal of our study is to propose new optimal pulsewidth modulation to achieve: low device switching frequency, minimal harmonic distortion of machine stator currents and elimination of zero-sequence currents. The main idea is to select the switching angles of two inverters such that zero-sequence components are eliminated and then perform optimization to determine switching angles that minimize the harmonic distortion of machine stator currents. The experimental results obtained from dual two-level and dual three-level inverter fed 1.5-kW open-end stator winding IM drive demonstrated the effectiveness of proposed modulation technique.**

***Index Terms*—Multilevel converters, synchronous optimal pulsewidth modulation, low device switching frequency, open-end stator winding induction motor.**

I. Introduction

MULTILEVEL converters (MLCs) have emerged as popular choice for medium voltage (MV) high power applications due to several obvious advantages [1]–[8]. The popular multilevel converter topologies are neutral-point or diode-clamped converters (NPC), flying-capacitor converters (FC) and cascaded H-Bridge converters (CHB). In addition, the concept of multilevel topology with dual two-level (D2L) inverter configuration feeding an open-end stator winding induction motor drive has been introduced for MV high power applications [9]. With this topology, it is possible to achieve three-level (3L) operation with half of dc-link voltage and without any neutral-point fluctuations compared to 3L-NPC topology. Similarly, dual three-level (D3L) inverter configuration with a single dc-link voltage was proposed for five-level (5L) operation [10]. Subsequently, several multilevel topologies have been proposed for open-end stator winding induction motor drives [11]–[14].

The major advantage of dual-inverter topologies over other topologies is minimal requirement of dc sources, which becomes obvious when number of voltage levels becomes more than three. For example, a 5L dual inverter topology requires a single dc source, whereas NPC and CHB based 5L topologies requires three and six isolated dc sources, respectively. Similarly, a 9L dual-inverter topology requires two dc sources [14], whereas NPC and CHB based 9L topologies require six and twelve isolated dc sources, respectively. In general, isolated dc sources are obtained from phase-shifting transformers, which are more bulky and expensive, compared to standard transformers required for dual-inverter topologies. However, these benefits of dual-inverter topologies come at the expense of additional cabling requirements for open-end stator winding induction motor drives. Additional merit of dual-inverter fed drives is availability of higher redundant switching state combinations compared to single-inverter fed drives of same output voltage levels. For example, D2L inverter has 64 space vector combinations, whereas 3L-NPC inverter has 27 space vector combinations to generate 19 space vector locations [15]. By utilizing these redundant space vectors, it is possible to achieve floating capacitor voltages balance, elimination of common-mode voltages and so on. Another advantage of dual-inverter topologies is that the voltage amplitude required to produce air-gap flux in the machine is divided among the two inverters. Therefore, the device ratings as well as $\frac{dv}{dt}$ stress are reduced, which is very important for high-power applications. The main disadvantage of dual-inverter topologies is requirement of common-mode inductor in series with machine phase windings to suppress the zero-sequence or common-mode current components.

In MV high power drives, energy efficiency is significantly improved by reducing the device switching frequency, which brings down the dominating switching losses. However, reducing the device switching frequency increases the total harmonic distortion (THD) of machine stator currents. In addition, it is important to eliminate the zero-sequence current components in dual inverter fed induction motor drives. Therefore, the challenge is to operate MLCs at low device switching frequencies, while eliminating zero-sequence current components and minimizing the THD of machine stator currents. In literature, space vector modulation (SVM) techniques have been proposed for D2L inverter fed open-end stator winding induction motor drives, for elimination of zero sequence currents as well as elimination of common mode voltages (CMV) which lead to bearing and leakage currents [16]-[17]. Later, SVM based CMV elimination techniques have been demonstrated for 5L and seven-level (7L) dual inverter topologies [18]-[19]. Also, pulse-width modulated (PWM) based scheme has been proposed for D2L inverter to reduce zero-sequence current by reducing the zero-sequence voltage to zero, in the average sense, within a sampling time interval [20]. A decoupled PWM scheme has been suggested

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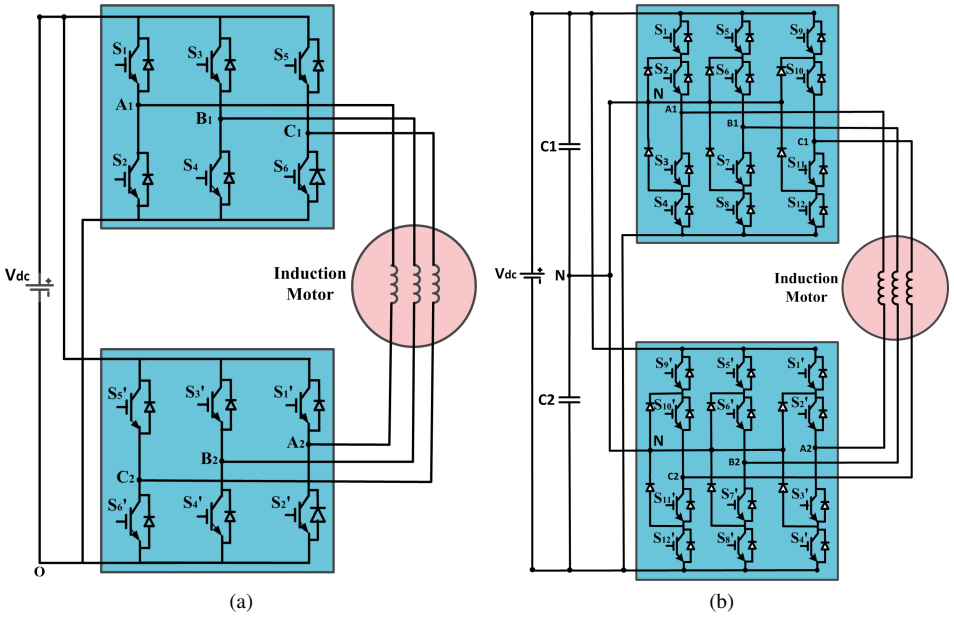

Fig. 1. Single dc-link dual inverter fed open-end stator winding induction motor drive. (a) D2L inverter (b) D3L inverter

for D2L inverter to reduce the current ripple [21]. However, all these modulation techniques require higher device switching frequencies (around 1 kHz) and hence, not preferred for MV high power drives.

Synchronous optimal pulsewidth modulation (SOP) is an emerging control technique to achieve low device switching frequency, while maintaining minimal harmonic distortion of machine stator currents [22]. It is an off-line optimization technique to determine switching angles that minimize the THD of machine stator currents. Because the calculations are done off-line for each steady-state operating point, the switching patterns are suitable only for low performance MV drives which operate in open-loop V/f control mode. For drives with high dynamic performance requirements, SOP should be combined with stator flux trajectory tracking control method [23]-[24] or model predictive control [25].

The SOP technique has been demonstrated for D3L inverter fed open-end stator winding induction motor drive with maximum device switching frequency limited to 200 Hz [26]. Subsequently, this SOP technique has been improved to minimize zero-sequence currents by using additional constraint 'VoltSecT' in the optimization [27]. However, the requirement of common-mode inductor still remains and its kVA-rating depends on the CMV at six-step operation. Therefore, the goal of our study is to propose a new SOP technique to achieve low device switching frequency with minimal THD of stator currents as well as elimination of zero-sequence currents. The idea is to impose a constraint on switching angles such that zero-sequence voltage components are eliminated and then, perform optimization to determine switching angles that minimize the THD of stator currents [28].

The multilevel topologies of D2L and D3L inverters feeding an open-end stator winding induction motor drive are shown in Fig. 1(a)-(b), respectively. In case of D2L inverter, two voltage levels $(V_{dc}, 0)$ are obtained between mid-point of each leg and negative terminal of dc-link capacitor 'O' and hence, three voltage levels $(-V_{dc}, 0, V_{dc})$ are obtained across each stator winding. In case of D3L inverter, three voltage levels $(-V_{dc}, 0, V_{dc})$ are obtained between mid-point of each leg and neutral-point of dc-link capacitors 'N' and hence, five voltage levels $(-2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc})$ are obtained across each stator winding.

The paper is organized as follows: Details of proposed SOP technique are given in Section II, and the experimental results are demonstrated in Section III to validate the proposed modulation technique.

II. Proposed Synchronous Optimal Pulsewidth Modulation

SOP technique is an off-line optimization based method to determine switching angles, which minimize the THD of machine stator currents. The word 'synchronous' is used because device switching frequency f_s is always made an integer multiple of motor fundamental frequency f_1. The induction motor is controlled using constant V/f control technique. The modulation index m is defined as f_1/f_{1R}, where f_{1R} denotes the rated fundamental frequency of induction motor (50/60 Hz). With half-wave and quarter-wave symmetries in the switching patterns, it is sufficient to know switching angles in a quarter period and also, all even order harmonics are eliminated. The total number of switching angles in a quarter period is denoted as pulse number N. Each steady-state operating point is denoted by (m, N). The first step in SOP technique is to compute the pulse number N for a given m such that f_s is limited to $f_{s,max}$. In second step, switching angles are selected such that zero-sequence voltages in three-phase windings are eliminated and later, optimization is conducted to determine switching angles that minimize the THD of machine stator currents for each steady-state operating point (m, N).

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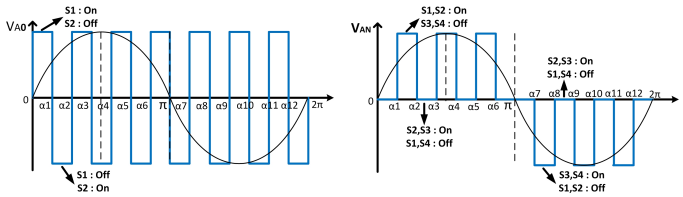


(a) (b)

Fig. 2. Output potential waveforms of (a) 2L inverter (b) 3L-NPC inverter

A. Computation of pulse number N

The output potential waveforms of 2L and 3L-NPC inverters are shown in Fig. 2(a)-(b), respectively. The pulse number for 2L and 3L-NPC inverters is denoted as N_{2L} and N_{3L}, respectively. For a 2L inverter, the total number of switching angles in one fundamental cycle of output voltage is equal to $4N_{2L}+2$. For example, it should be observed from Fig. 2(a) that N_{2L} is equal to 3, i.e., $\alpha1$ to $\alpha3$ and the total number of switching angles are equal to 14, i.e., 0, π, $\alpha1$ to $\alpha12$. At each switching angle, both the semiconductor devices in a phase leg undergo commutation, for example, S_1 is turned off and S_2 is turned on at $\alpha1$, as shown in Fig. 2(a). Therefore, the total number of commutations of each semiconductor device are equal to $4N_{2L}+2$ and hence, the device switching frequency f_s of the 2L inverter is equal to $(2N_{2L}+1)f_1$. For a 3L-NPC inverter, the total number of switching angles in one fundamental cycle is equal to $4N_{3L}$. For example, it is observed from Fig. 2(b) that N_{3L} is equal to 3, i.e., $\alpha1$ to $\alpha3$ and the total number of switching angles are equal to 12, i.e., $\alpha1$ to $\alpha12$. At each switching angle, only two switches in a phase leg undergo commutation. For example, S_1 is turned off and S_3 is turned on at $\alpha2$, whereas S_2 is turned on and S_4 is turned off at $\alpha8$, as shown in Fig. 2(b). Therefore, total number of commutations of each semiconductor device is equal to $2N_{3L}$ and hence, the device switching frequency f_s of the 3L-NPC inverter is equal to $N_{3L}f_1$. Then, the values of N_{2L} and N_{3L} for a desired maximum device switching frequency $f_{s,max}$ are obtained as,

$$N_{2L} = floor\left(\frac{f_{s,max}-f_1}{2f_1}\right) = floor\left(\frac{f_{s,max}-mf_{1R}}{2mf_{1R}}\right) \quad (1)$$

$$N_{3L} = floor\left(\frac{f_{s,max}}{f_1}\right) = floor\left(\frac{f_{s,max}}{mf_{1R}}\right). \quad (2)$$

The pulse number for D2L inverter (N_{D2L}) and D3L inverter (N_{D3L}) is equal to $2N_{2L}$ and $2N_{3L}$, respectively. The goal is to operate D2L and D3L inverters with maximum device switching frequency $f_{s,max}$ limited to 400 Hz and 200 Hz, respectively. Based on (1) or (2), pulse number for D2L and D3L inverters can be determined such that device switching frequencies are limited to $f_{s,max}$. For D2L and D3L inverters, pulse number and device switching frequency f_s for a given m are shown in Table I (a)-(b), respectively. The device switching frequency f_s versus motor fundamental frequency f_1 for D2L and D3L inverters is shown in Fig. 3 (a)-(b), respectively. It should be observed from Table I and Fig. 3 that $f_{s,max}$ for D2L and D3L inverters is limited to 400 Hz and 200 Hz, respectively. After determining the values of N_{D2L} and N_{D3L} for a given m, the next step is to determine optimal switching angles for each steady-state operating point.

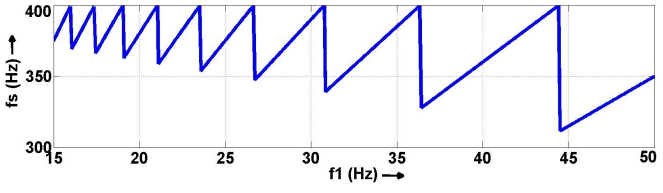
Table I: Pulse number N and device switching frequency f_s for a given m. (a) D2L inverter (b) D3L inverter

m	$f_1(Hz)$	N_{2L1}	N_{2L2}	N_{D2L}	f_s(Hz)
0.889 - 1.000	44.49 - 50.00	3	3	6	311.46 - 350
0.728 - 0.888	36.41 - 44.44	4	4	8	327.73 - 400
0.616 - 0.727	30.82 - 40.00	5	5	10	339.01 - 400
0.534 - 0.615	26.72 - 30.77	6	6	12	347.32 - 400
0.471 - 0.533	23.58 - 26.67	7	7	14	353.69 - 400

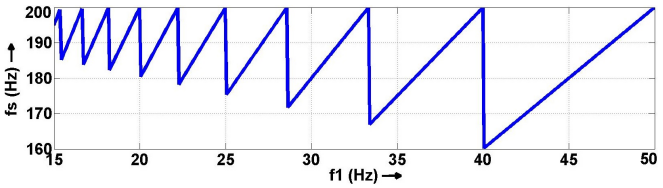
(a)

m	$f_1(Hz)$	N_{3L1}	N_{3L2}	N_{D3L}	f_s(Hz)
0.801 - 1.000	40.05 - 50.00	4	4	8	160.20 - 200
0.667 - 0.800	33.38 - 40.00	5	5	10	166.90 - 200
0.572 - 0.667	28.62 - 33.33	6	6	12	171.73 - 200
0.501 - 0.571	25.05 - 28.57	7	7	14	175.35 - 200
0.445 - 0.500	22.27 - 25.00	8	8	16	178.17 - 200

(b)



(a)



(b)

Fig. 3. Device switching frequency f_s versus motor fundamental frequency f_1. (a) D2L inverter (b) D3L inverter

B. Derivation of Objective Function

The distortion factor d is used as an objective function for optimization, which is independent of machine parameters. The expression of d is given by [29],

$$d = \frac{i_h}{i_{h,six-step}} \quad (3)$$

where, i_h, $i_{h,six-step}$ represents the harmonic rms current during normal operation and six-step operation (m=1) of multilevel inverter, respectively. The stator winding voltage of D2L and D3L inverter fed induction motor drives consists of 3L and 5L waveforms, respectively. Using Fourier series analysis of machine phase voltages v_{j1j2} (j=A,B,C), the final

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expressions for d_{D2L} and d_{D3L} is obtained as [28],

$$d_{D2L} = \frac{\sqrt{\sum_k (\frac{1}{k^4})(\sum_{i=1}^{N_{D2L}} s(i)cos(k\alpha_i))^2}}{\sqrt{\sum_k (\frac{1}{k^4})}} \quad (4)$$

$$d_{D3L} = \frac{\sqrt{\sum_k (\frac{1}{k^4})(\sum_{i=1}^{N_{D3L}} s(i)cos(k\alpha_i))^2}}{2\sqrt{\sum_k (\frac{1}{k^4})}} \quad (5)$$

where, k corresponds to k^{th} order harmonic (k=1,5,7,9,11...) and term $s(i)$ represents the slope of switching transition at switching angle α_i. The value of $s(i)$=1 when v_{j1j2} switches to higher potential and $s(i)$=-1 when v_{j1j2} switches to lower potential. Because the induction motor is operated in constant V/f control mode, the constraint on switching angles to set the fundamental frequency of inverter output voltage to f_1 is obtained as,

$$m_{D2L} = \sum_{i=1}^{N_{D2L}} s(i)\cos(\alpha_i) \quad (6)$$

$$m_{D3L} = \frac{1}{2}\sum_{i=1}^{N_{D3L}} s(i)\cos(\alpha_i) \quad (7)$$

C. Elimination of zero-sequence currents

The zero-sequence currents are due to zero-sequence or common-mode voltages in the machine stator windings. A common-mode inductor is usually required in series with stator windings to suppress zero-sequence components. Let $CMV1$, $CMV2$ represents the common-mode voltages generated by first inverter $inv1$ and second inverter $inv2$, respectively. If the switching patterns are selected such that $CMV1$ = $CMV2$, then common-mode voltages become zero in the phase windings and hence, zero-sequence current components are eliminated. For a 2L inverter, the voltage space vectors for different switching combinations are shown in Fig. 4. It can be observed that, common-mode voltages generated by voltage space vectors 1, 3 and 5 that are 120° phase apart, are equal to $\frac{V_{dc}}{3}$. Similarly, the common-mode voltages generated by voltage space vectors 2, 4 and 6 that are 120° phase apart, are equal to $\frac{2V_{dc}}{3}$. Therefore, by choosing the switching combinations for $inv1$ and $inv2$ that are 120° phase apart, it is possible to cancel the common-mode voltages generated across the phase windings. For example, if the switching combinations for $inv1$ and $inv2$ correspond to space vectors 1 and 3, respectively, then common-mode voltages generated across the phase winding will be equal to zero. Another way of understanding is that, the zero-sequence voltage components consist of third order harmonic components and hence, they can be eliminated by maintaining 120° phase-shift between the inverter output voltages.

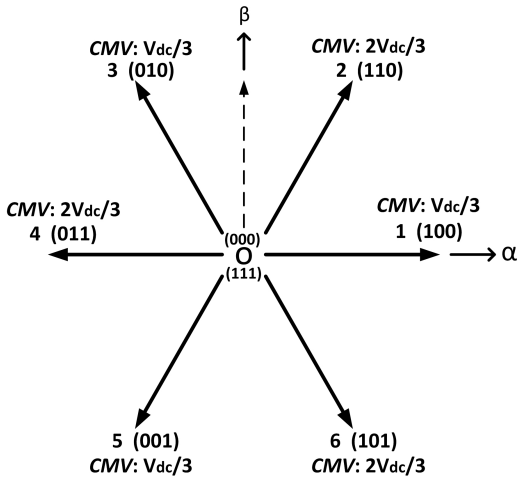

Fig. 4. Voltage space vectors for two-level inverter

D. Optimization Algorithm

The optimization algorithm is implemented using MATLAB. The gradient method through 'FMINCON' function with active-set algorithm available in MATLAB is used for searching switching angles α_i (i = 1 to N) that minimize the objective function d. The switching angles are subjected to non-linear constraint given by (6) or (7) and two linear constraints : $0 < \alpha_i < \pi/2$ and $\alpha_{i+1} - \alpha_i < m.\theta$, where θ is a fixed value which define the minimum on-time and off-time (e.g. 10 μs) of semiconductor devices. The iterations stop when change in the value of objective function $\Delta d < 10^{-15}$. Only harmonic components up to order of 100 are considered. The flow-chart of the optimization algorithm is shown in Fig. 5. The details of optimization algorithm are given next.

1) Determine the pulse number N: The value of N for a given m is obtained based on (1) or (2), as shown in Table I

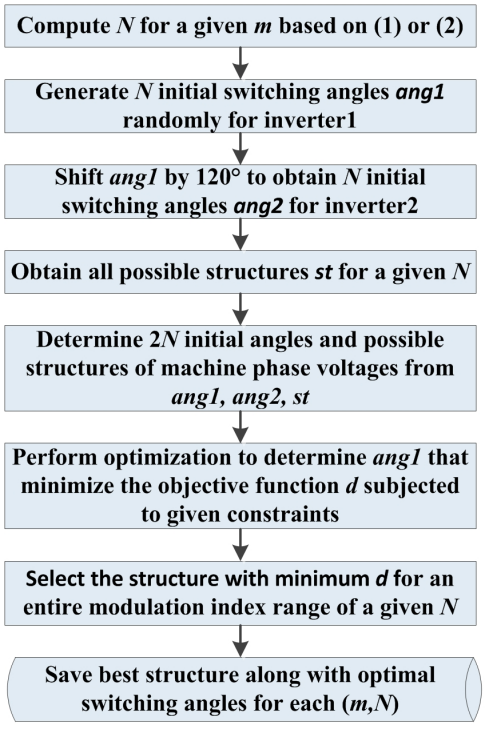

Fig. 5. Flow chart of proposed SOP algorithm for dual inverter fed open-end winding induction motor drives

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(a)-(b). It can be observed that the value of N remains same for a range of modulation index values.

2) Initialization: During initialization, it should be ensured that the switching angles correspond to a given modulation index m. Initially, MATLAB function 'randn' is used to generate the random switching angles α_2 to α_N with mean zero and standard deviation equal to one. The switching angle α_1 is calculated to satisfy the relation (6) or (7). The complete initialization procedure for a given operating point (m, N) is as follows : generate a set of N initial switching angles $ang1$ randomly for one inverter and then, obtain another set of initial switching angles $ang2$ for other inverter by shifting $ang1$ by 120°. Next, possible structures st of inverter output voltages (2L or 3L) are determined. The structure of an inverter output represents sequence of voltage levels and is usually represented by switching transitions at each switching angle [30]. For example, 2L and 3L waveforms have only one possible structure, as shown in Fig. 2. Finally, a set of initial switching angles and possible structures for stator voltages are determined.

3) Optimization: The goal of optimization is to determine the switching angles that minimize the distortion factor given by (4) or (5) for each steady state operating point. The optimization is done for all possible structures of a given operating point (m, N), starting from initial switching angles obtained in previous step. The structure which exhibits minimum d over a modulation index range correspond to a given pulse number N is recorded. The optimal switching patterns consists of optimal switching angles along with switching transitions $s(i)(i = 1$ to $N)$ of the best possible structure. After optimization, it might happen that switching angles for consecutive operating points with same pulse number N differ by large values. This leads to transients in machine currents whenever the operating point passes a point of discontinuity. Therefore, post-optimization is required to establish the continuity of switching angles for an entire modulation index range of a given pulse number N [31].

E. Optimization Results

The optimal switching angles were determined for D2L and D3L inverters with $f_{s,max}$ limited to 400 Hz and 200 Hz, respectively. The results of proposed SOP technique for D2L and D3L inverters for different values of m are shown in Fig. 6. It should be observed that the performance of a D3L inverter is always better than a D2L inverter due to higher number of voltage levels. The best performance is achieved in the range from m = 0.30 to 0.94. As the value of m approaches close to unity, the inverter operation reaches six-step operation. The performance of optimization reduces at lower m and hence, SVM is preferred when $m \leq 0.3$ [26]. However, high power drives are usually operated in the higher modulation index range $(m > 0.5)$, where SOP offers superior performance.

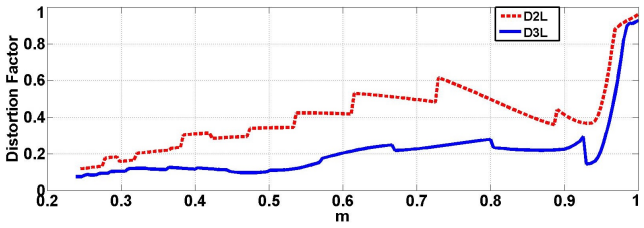

Fig. 6. Results of optimization for D2L and D3L inverters : d versus m

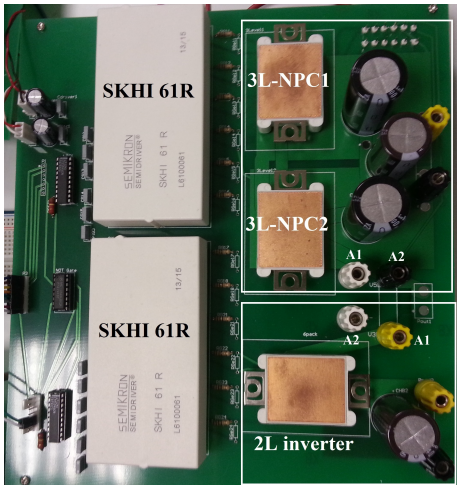

Fig. 7. Prototype of D2L and D3L inverters for one of the three phases

Table II: List of components and their parameters in the experimental setup

Components	Parameters
Induction Motor	QCAVM 90 S 1.5 kW, 400 V, 50 Hz, 1500 RPM
3-level Module	F3L30R06W1E3_B11 V_{CE} =600 V, I_{Cnom} =30 A
Six-pack Module	FS30R06W1E3 V_{CE} =600 V, I_{Cnom} =30 A
Six-pack Driver	SKHI 61R V_{CE} =900 V, f_{max} =50 kHz

III. Experimental Results

The proposed SOP technique is implemented for modulating D2L and D3L inverters feeding an 1.5-kW open-end stator winding induction motor drive. Experimental laboratory prototype of D2L and D3L inverters for one of the three phases is shown in Fig. 7. The list of components and their parameters are shown in Table II. The DC input voltages to D2L and D3L inverters are maintained at 70 V and 60 V, respectively. The output of D2L and D3L inverters is directly connected to induction motor without using any filter to get better understanding of significant harmonics in machine stator currents with optimal switching patterns. The induction motor is coupled to a separately excited DC generator and its output is connected to a fixed resistive load.

A. D2L Inverter

SOP technique generated optimal switching angles for three operating points (m=0.9333, f_1=46.67 Hz, N=6), (m=0.7255, f_1=36.275 Hz, N=10) and (m=0.5020, f_1=25.1 Hz, N=14). For each operating point, the machine stator winding voltage, stator current, and zero-sequence current are shown in Fig. 8 (a)-(c), respectively. The phase voltages consists of 3L waveforms

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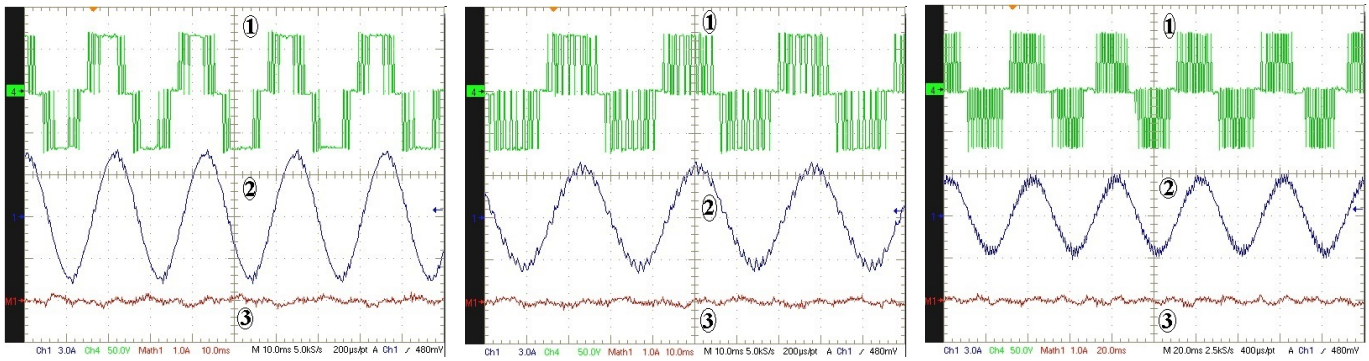
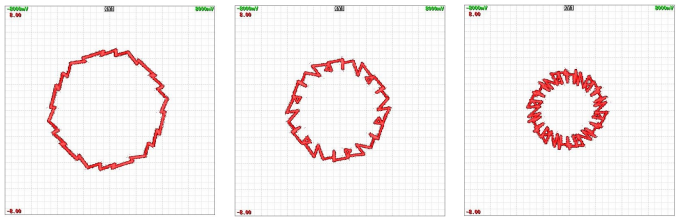


(a) (b) (c)

Fig. 8. (a) Experimental results for (m=0.9333, N=6). X-axis:10 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div). (b) Experimental results for (m=0.7255, N=10). X-axis:10 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div). (c) Experimental results for (m=0.502, N=14). X-axis:20 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div)



(a) (b) (c)

Fig. 9. Stator current space vector trajectories for D2L inverter. X-axis, Y-axis: 2 A/div (a) (m=0.9333, N=6) (b) (m=0.7255, N=10) (c) (m=0.5020, N=14)

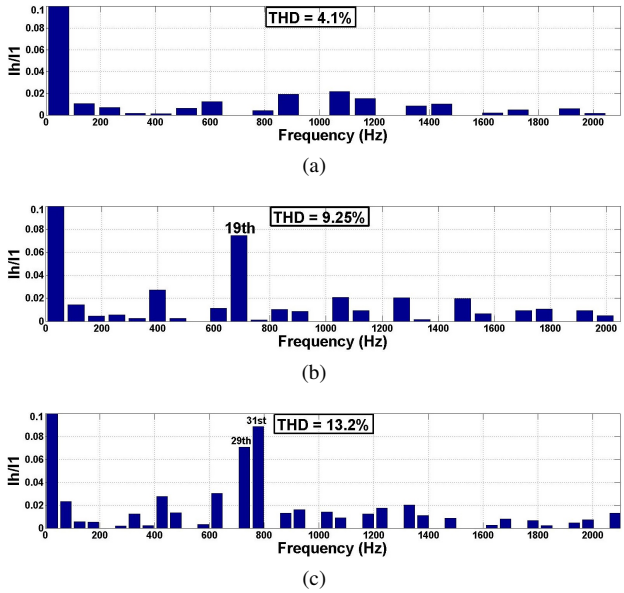


Fig. 10. Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Frequency (Hz). Y-axis: $\frac{I_h}{I_1}$. (a) (m=0.9333, N=6) (b) (m=0.7255, N=10) (c) (m=0.502, N=14)

and stator currents are sinusoidal. The zero-sequence current components are calculated by using relation $(i_a + i_b + i_c)/3$ and it can be observed that they are almost eliminated.

The space vector trajectories of stator currents corresponding to three operating points are shown in Fig. 9 (a)-(c), respectively. The nearly circular trajectories demonstrate low THD, while device switching frequencies are limited to 400 Hz. It can be observed that harmonic distortion increases at lower values of modulation index. In addition, FFT analysis is performed on stator currents recorded into a PC by using data acquisition system. The current harmonic spectrum for operating point (m=0.9333, N=6) is displayed in Fig. 10(a). It can be observed that THD of stator currents is equal to 4.1% with all the significant harmonics below 2% of fundamental. For operating point (m=0.7255, N=10), THD of stator currents is equal to 9.25% as shown in Fig. 10(b) with one significant harmonic (19^{th}) of magnitude equal to 7.5% of fundamental. Similarly, for operating point (m=0.502, N=14), THD of stator currents is equal to 13.2% as shown in Fig. 10(c) and there are two significant harmonics (29^{th} and 31^{st}) with magnitude equal to 7% and 8.9% of fundamental. The THD of stator currents seems significant for operating point (m=0.5020, N=14), but this is due to harmonics of higher order, which can be attentuated easily by using LC filter at the inverter output.

B. D3L Inverter

To demonstrate the performance of proposed SOP technique, three operating points (m=0.9294, f_1=46.47 Hz, N=8), (m=0.6667, f_1=33.33 Hz, N=12) and (m=0.5098, f_1=25.49 Hz, N=14) were selected. For each operating point, the machine stator winding voltage, stator current, and zero-sequence current are shown in Fig. 11 (a)-(c), respectively. The stator voltage consists of 5L waveforms and stator currents are sinusoidal. The improvement in THD of stator currents compared to D2L inverter can be observed. The zero-sequence current components are almost eliminated. It should be noted that, the stator currents in each phase might differ in magnitude due to unequal winding resistances and inductance values and hence, there exist small zero-sequence current.

The space vector trajectories of stator currents corresponding to three operating points, are shown in Fig. 12 (a)-(c), respectively. The nearly circular trajectories demonstrate low THD, while maximum device switching frequencies were limited to 200 Hz. In addition, data acquisition system was used to record stator currents into a PC and FFT analysis was performed. It can be observed from Fig. 13 (a)-(c) that the

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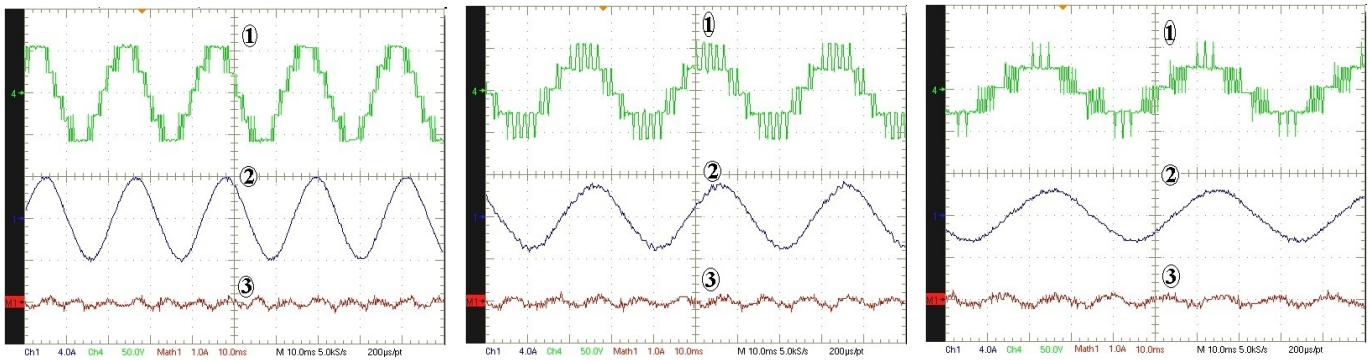
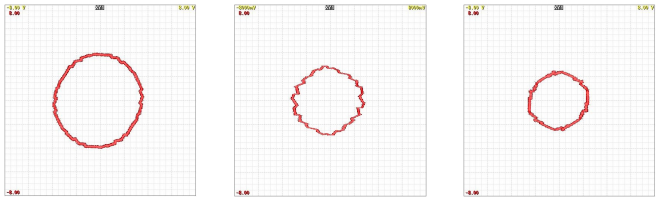


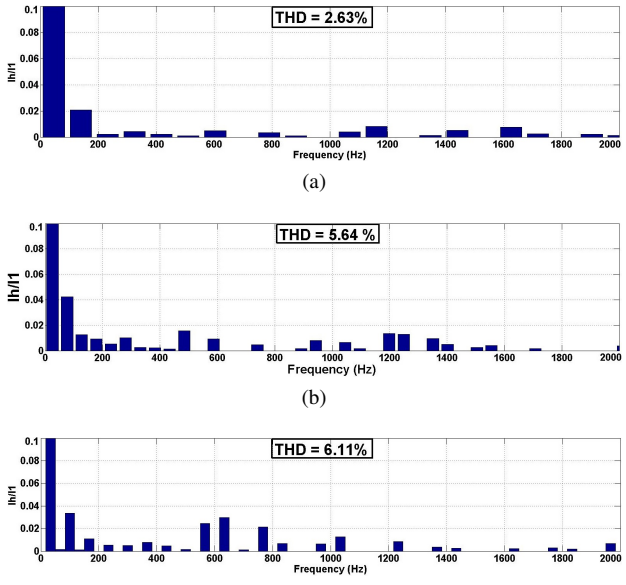
(a) (b) (c)

Fig. 11. (a) Experimental results for (m=0.9294, N=8). X-axis:10 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div). (b) Experimental results for (m=0.6667, N=12). X-axis:10 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div). (c) Experimental results for (m=0.5098, N=14). X-axis:10 ms/div. (1) Machine stator voltage (Y-axis:50 V/div). (2) Stator current (Y-axis:4 A/div). (3) Zero-sequence current (Y-axis:1 A/div)



(a) (b) (c)

Fig. 12. Stator current space vector trajectories for D3L inverter. X-axis, Y-axis: 2 A/div (a) (m=0.9294, N=8) (b) (m=0.667, N=12) (c) (m=0.5098, N=14)



(a) (b) (c)

Fig. 13. Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Frequency (Hz). Y-axis: $\frac{I_h}{I_1}$. (a) (m=0.9294, N=8) (b) (m=0.667, N=12) (c) (m=0.5098, N=14)

THD of stator currents for three operating points are equal to 2.63%, 5.64% and 6.11%, respectively. Due to 5L stator voltage waveforms in D3L inverter, better quality of stator current waveforms are achieved even with half of the device switching frequency compared to D2L inverter.

IV. Summary and Conclusion

Dual inverter configurations for open-end winding induction motor drives requires common mode inductor to suppress the zero-sequence currents. Also, medium voltage high power drives require low device switching frequency with high quality of machine stator currents. Therefore, a new synchronous optimal pulsewidth modulation (SOP) has been proposed to achieve minimal harmonic distortion of machine stator currents and elimination of zero-sequence currents, while operating semiconductor devices at low switching frequency. The proposed SOP technique has been demonstrated on D2L and D3L inverters fed open-end stator winding induction motor drive with $f_{s,max}$ limited to 400 Hz and 200 Hz, respectively. In case of D2L inverters, the zero-sequence components are almost eliminated with THD of machine currents varying from 4% to 13%. Moreover, significant harmonics in current waveforms are of high order which can be further attenuated by using LC filter at the inverter output terminals. The D3L inverter has better current waveforms with THD of stator currents varying from 2% to 7%, while $f_{s,max}$ is limited to 200 Hz because of higher number of voltage levels comapared to D2L inverter.

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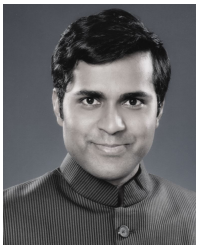

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