This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

Ripple Minimization Through Harmonic Elimination in Asymmetric Interleaved Multiphase dc-dc Converters

Marcel Schuck, *Student Member, IEEE*, Robert C.N. Pilawa-Podgurski, *Member, IEEE*

Part of this manuscript was presented at the IEEE Energy Conversion Congress and Exposition (ECCE), September 2013 in Denver, Colorado.

***Abstract*—Symmetric multiphase dc-dc converters are widely used in power electronics, as they enable the processing of high power through splitting the overall load-current into multiple phases. Distributing the processed power symmetrically between the phases and performing ripple minimization through interleaving is well understood. However, in recent applications such as maximum power point (MPP) tracking for solar photovoltaic (PV), converters are forced to operate under asymmetric conditions, due to differences in the sources or loads of each converter. This work presents a control technique, based on harmonic elimination, that allows for ripple minimization under asymmetric conditions. The mathematical derivations are outlined and simulations are used to evaluate the performance of the proposed technique. Measurements taken from an experimental prototype, consisting of three dc-dc buck converters, demonstrate significant improvements in ripple reduction over conventional interleaving techniques. When the multi-phase converter is operated at the optimum asymmetric phase-shift found through the techniques presented here, a more than 3x reduction in net current ripple is observed under realistic operating conditions. Additionally, the undesirable first harmonic ripple component is reduced by 14.8 dB with the proposed technique.**

***Index Terms*—multiphase converter, interleaved converter, asymmetric operation, harmonic elimination, ripple minimization.**

I. Introduction

CURRENT ripple cancellation is an important feature of multiphase switching converters, as it enables each individual converter of the system to operate at a higher ripple than the overall load-current ripple through interleaving of the phases [1]–[4]. This yields significantly lower values for the inductor and capacitors of each converter, and (as shown in [5], [6]) it can lead to substantial reductions in converter size and cost, while increasing the efficiency. In standard symmetric multiphase converters (see Fig. 1), where the output current is the sum of all phase currents, it is possible to accomplish a load-current ripple minimization by phase-shifting the switching functions of each phase by an angle determined by

$$\phi_n = (n-1) \cdot \frac{360^\circ}{N}, \tag{1}$$

Marcel Schuck is with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, CH-8092, Zurich, Switzerland. At the time the presented research was carried out, he was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign. Robert C. N. Pilawa-Podgurski is with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL, 61801, USA. E-mail: pilawa@illinois.edu

where N is the total number of phases and n is the considered phase [7]–[10]. This technique is well understood and described in power electronics literature [11] for a balanced operation of all parallel phases with a common source and a common load. Recently, asymmetric phase-shifting has been used to account for imbalances in the converter phases due to component tolerances [12]–[14], and in the context of EMI noise shaping, where certain higher order harmonics can be reduced, which therefore reduces the filter size as dictated by EMI regulations [15]–[17]. This method is also employed in multilevel cascaded H-bridges with non-equal dc-link voltages to reduce sideband harmonics [18], [19]. However, as demonstrated in [12], [13], little improvement can be achieved due to practical limitations such as measurement errors and signal delays in the complex control circuitry. Usually, component tolerances are small, which means that the deviations from symmetrical operation are limited. Consequently, the additional cost introduced by the more sophisticated control might not be justified. Contrarily, phase-shifting for non-uniform duty ratios and different input sources for each phase is a more relevant field of application for these techniques, that is not well understood, and has not been explored in the literature. Figure 3 shows a schematic drawing of an emerging application where non-uniform duty ratios occur. A single PV panel is usually divided into three sub-modules, which are connected to separate inputs of the converters. Each power converter performs MPP tracking for one sub-module. The MPP of a PV cell varies with irradiation and temperature. It may also change throughout the lifetime of a cell due to aging. Figure 4 shows the variation of the MPP and the change in the respective voltage V_{MPP} for different levels of irradiation in the case of a single PV cell. As has been shown, operating individual panels [11], or even sub-modules [20]–[23] at their individual MPPs, can yield a significant improvement in energy capture in PV applications. In addition to the aforementioned references, possible implementations and the corresponding control of distributed maximum power point tracking (DMPPT) are also presented in [24]–[28]. The topology shown in Fig. 2 is used as an example in this paper. MPP tracking is performed locally on a sub-module level through a dc-dc converter that is connected to a string of solar cells at its input. The global maximum power point tracking is done by the inverter and can be performed on different levels, e.g. for all panels, a single string, or a single panel. In the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

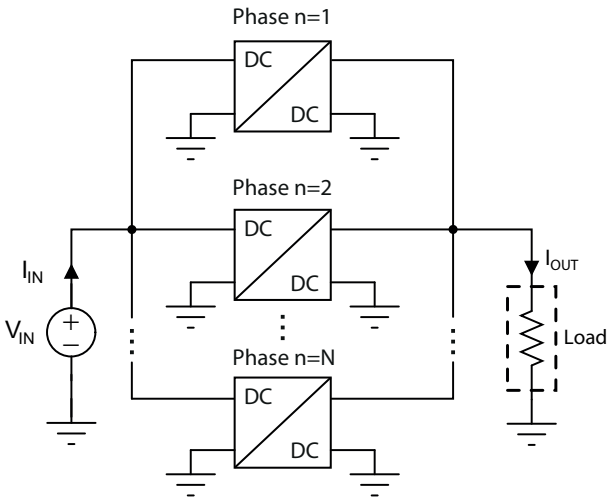


Fig. 1: Standard multi-phase interleaved converter topology with common input and output voltages.

system of Fig. 3, all the outputs of the dc-dc converters are connected in series - supplying one common load. However, since the operating point of each sub-module may differ due to shading, manufacturing tolerances, cell damage, and aging; the duty cycles of the individual converters are oftentimes different. These operating conditions are different from what is usually referred to as multi-phase interleaved converters as described above. The average output current is identical for all three converters, but the output voltages are different due to the series connection. In this application, it is desirable to employ interleaving of the module (or sub-module) converters to reduce the overall current ripple, and enable the use of small, low-cost inductors in each converter. This is still possible, because of the common output current. Furthermore, the DMPPT converters do not require large electrolytic capacitors, as they do not need to buffer the line-frequency power ripple. This ripple is buffered by the inverter, which is connected to the output of the dc-dc converters. The dc input ripple is typically buffered by PV interfacing circuits in modern grid-connected PV inverters [29].

Interleaving of the different converters and applying a symmetric phase-shift will yield some benefits in the architecture of Fig. 3. However, methods that go beyond this technique are required to *minimize* the output current ripple under asymmetric operating conditions, which will be explored in this work. The presented results are universally applicable for different dc-dc converter topologies, such as buck-type (buck, buck-boost, flyback) and boost-type (boost, boost-buck, SEPIC) converters. This work represents an expansion of our earlier conference paper [30], and includes a more detailed description of the proposed control method, as well as additional discussions and more extensive experimental results.

The remainder of this paper is organized as follows: Section II presents the mathematical derivation of the proposed ripple cancellation method for asymmetric converter operation, and Section III describes a control technique that can be applied together with an MPP tracking algorithm. Section IV provides simulation results that illustrate the improvement that

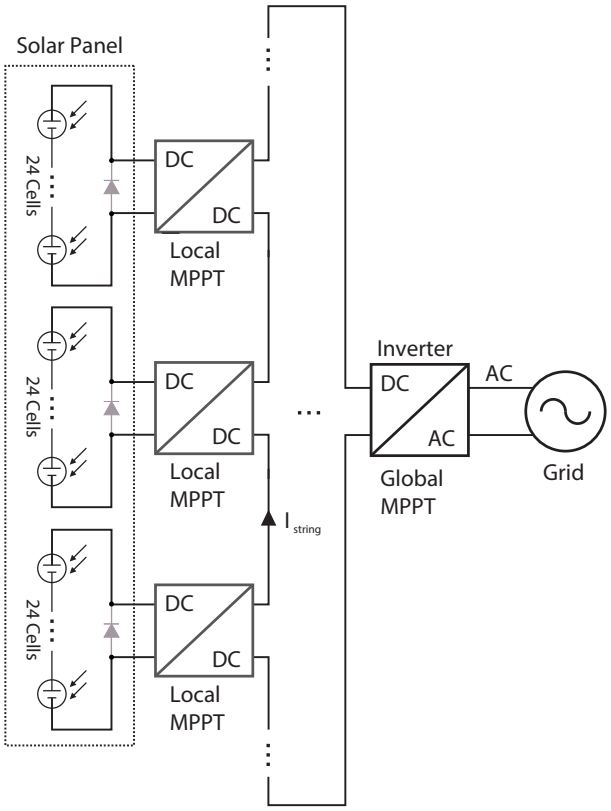


Fig. 2: DMPPT topology used as an example in this work.

is achievable with the proposed method compared to a conventional phase-shifting technique. The results are verified in Section V by applying the proposed control to an experimental prototype. Finally, Section VI summarizes and concludes the paper.

II. Mathematical Description of the Problem

The previous section provided numerous examples in the literature [1]–[11] that describe standard interleaved multi-phase converters in different applications. Additionally, asymmetric phase-shifting techniques have recently been proposed to compensate for component tolerances [12]–[14], and a number of different applications for these techniques have been proposed in [15]–[17]. This paper extends the aforementioned works to the general case of different operating points for the converter of each phase in multiphase circuits. This will facilitate ripple minimization in DMPPT applications such as described in [20]–[28]. Our previous work in this area can be found in [30]–[33]. A key contribution of our proposed analysis technique is that it is based on a more universally applicable frequency-domain description of the converter current waveforms, as opposed to a time-domain description as outlined in [34], [35]. References [36]–[38] describe the mathematical fundamentals of the presented analysis.

A. Two Phases ($N = 2$)

For the case of two converter phases ($N = 2$), a 180° shift of the operation between phases yields the optimal cancellation effect. However, a complete cancellation of a certain harmonic

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

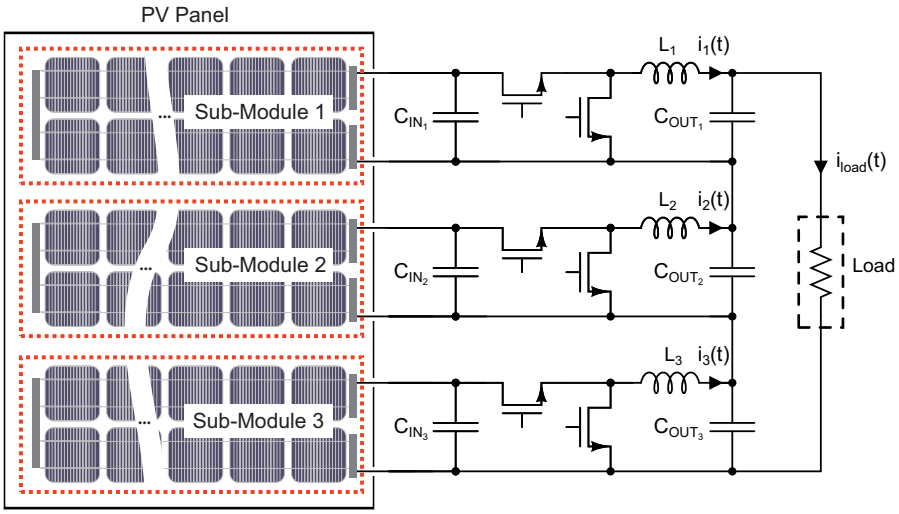


Fig. 3: Multiphase dc-dc buck converter in a solar PV application.

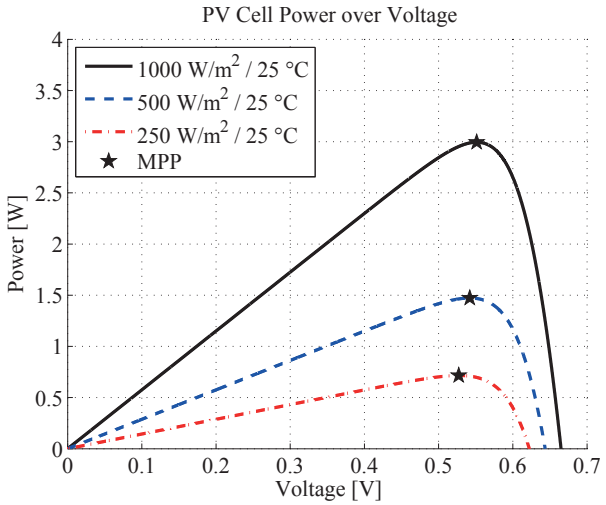


Fig. 4: Output power of a PV cell at different irradiation levels and constant temperature.

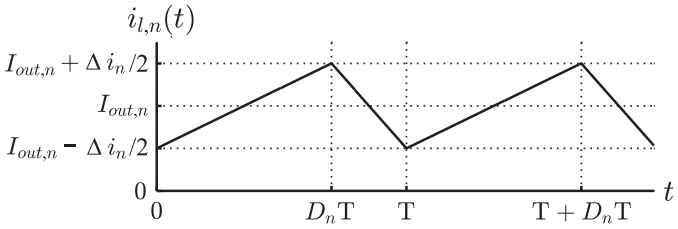


Fig. 5: Inductor current waveform for a buck converter in continuous conduction mode.

ripple component is not possible under asymmetric operating conditions.

The conditions for improved ripple cancellation in asymmetric multiphase circuits are derived for the case of general N here.

B. Derivations for general N

In multiphase dc-dc converters N current ripple waveforms can be observed where the shape varies depending on the converter type and operation mode (see [31] for an overview). The framework presented here is universally applicable and can be used for various converter types and modes of operation. As one illustrative example, consider the buck converter. Figure 5 shows the inductor current ripple waveform for buck-type converter topologies (buck, buck-boost, flyback) in continuous conduction mode (CCM). This waveform is used as an example in the derivations here. However, it should be noted that the general method presented here is applicable to other waveforms as well.

In the PV application considered here, each sub-module may operate at a slightly different voltage and current, owing to a mismatch in the I-V relationship between sub-modules. This mismatch can occur due to manufacturing variability, partial shading, aging, and dirt accumulation. The different input sources cause different magnitudes of the average output voltages $V_{out,n}$ in the output series-connected topology shown in Fig. 3. Moreover, different duty ratios D_n can be observed. The overall current ripple can be obtained by summing up all N ripple components, which are denoted by $\tilde{i}_n$

$$\tilde{i}_{sum}(t) = \sum_{n=1}^{N} \tilde{i}_n. \tag{2}$$

The magnitude of $\tilde{i}_{sum}(t)$ can be minimized by adequately phase-shifting the ripple components of the individual phases. The input voltages, input currents, output voltages, output currents, and duty ratios of all converters are determined by the operating conditions. Consequently, the phase shift is left as the only degree of freedom to influence the current ripple. To describe the waveform shown in Fig. 5 in terms of the phase-shift angle ϕ_{0n} of each phase, it is represented by its Fourier series. Performing the calculations in the frequency domain makes it possible to directly influence certain harmonic frequency components of the ripple, which are occurring at multiples of the switching frequency. This makes the proposed solution more universally applicable than a time-domain analysis such as outlined in [34], [35]. In practice,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

the goal is typically to minimize the lowest harmonics of the ripple, as they are usually dominant and dictate the output filter requirements.

In general, the Fourier series of the current waveform for each phase is obtained as

$$i_n(t) = \frac{a_{n0}}{2} + \sum_{k=1}^{\infty} \big[a_{nk} \cdot \cos(k(\omega t - \phi_{0n})) + ... \\ b_{nk} \cdot \sin(k(\omega t - \phi_{0n}))\big], \tag{3}$$

where n is the considered phase and k denotes the harmonic order.

An alternative representation based on the sum of phase-shifted cosine terms is given as

$$i_n(t) = \frac{a_{n0}}{2} + \sum_{k=1}^{\infty} A_{nk} \cdot \cos(k(\omega t - \phi_{0n}) - \varphi_{nk}) \tag{4}$$

with A_{nk} being the magnitude and φ_{nk} being the phase of the Fourier coefficient. The two forms are related by

$$A_{nk} = \sqrt{a_{nk}^2 + b_{nk}^2} \tag{5}$$

and

$$\varphi_{nk} = \mathrm{atan2}(b_{nk}, a_{nk}), \tag{6}$$

where $\mathrm{atan2}$ is the inverse tangent function that returns the angle in the interval of $(-\pi, \pi]$.

For the considered ripple components $\tilde{i}_n$ of the waveform shown in Fig. 5, the Fourier coefficients can be calculated as shown in the Appendix. The resulting Fourier coefficients are:

$$a_{n0} = 0 \tag{7a}$$

$$a_{nk} = 0 \tag{7b}$$

$$b_{nk} = -\frac{\Delta i_n (-1)^k}{k^2 D_n (1 - D_n) \pi^2} \sin\left[k(1 - D_n)\pi\right]. \tag{7c}$$

When applying the substitution

$$\theta_{nk} = k\phi_{0n} + \varphi_{nk}, \tag{8}$$

the expression inside the sum in Eq. (4) can equivalently be rewritten as a phasor

$$A_{nk} \cdot \mathrm{e}^{-j\theta_{nk}}. \tag{9}$$

Note that the following derivation can be simplified for the waveform shown in Fig. 5, as $a_{nk} = 0$ and therefore $A_{nk} = b_{nk}$ and $\phi_{nk} = \pm\frac{\pi}{2}$. However, it is carried out for the general case in order to be applicable to other waveforms.

Using Eq. (2), the summation of a certain harmonic ripple component corresponds to the summation of all phasors, whose magnitudes A_{nk} are determined by the converter operation. From the harmonic addition theorem [36], it is known that the sum of sinusoidal functions can again be written as a sinusoid. The goal of minimizing the harmonic ripple component dependent on the phase-shift angles ϕ_{0n} can therefore be achieved by minimizing the corresponding phasor sum

$$\min_{\theta_{nk}, n=[1,2,\ldots,N]} \left| \sum_{n=1}^{N} A_{nk} \cdot \mathrm{e}^{-j\theta_{nk}} \right|. \tag{10}$$

To minimize this cost function (absolute value of the summed phasor), its real and imaginary parts can be minimized separately. Moreover, $\theta_{1k} = 0$ can be chosen as a reference, which results in a purely real phasor corresponding to the first phase. The reformulated minimization problem is given by

$$\min_{\theta_{nk}, n=[2,\ldots,N]} \Bigg(\Bigg| \underbrace{A_{1k} + \sum_{n=2}^{N} A_{nk} \cdot \cos(\theta_{nk})}_{\text{real part}} \Bigg| + ... \\ \Bigg| \underbrace{\sum_{n=2}^{N} A_{nk} \cdot \sin(\theta_{nk})}_{\text{imaginary part}} \Bigg| \Bigg). \tag{11}$$

The complete cancellation of a certain harmonic component may be possible, depending on the magnitudes A_{nk}. In this case, the corresponding condition can be written as

$$\sum_{n=1}^{N} A_{nk} \cdot \mathrm{e}^{-j\theta_{nk}} = 0. \tag{12}$$

C. Analytic Solution for $N = 3$

A unique analytic solution can be found [30], [31] for the case where $N = 3$ as shown in the Appendix. The closed form analytic expressions for the relative phase-angles are as follows:

$$\phi_{01} = -\frac{\varphi_{1k}}{k} \tag{13a}$$

$$\phi_{02} = \frac{1}{k} \cdot \left[\cos^{-1}\left(\frac{-A_{1k}^2 - A_{2k}^2 + A_{3k}^2}{2A_{1k}A_{2k}} \right) - \varphi_{2k} \right] \tag{13b}$$

$$\phi_{03} = \frac{1}{k} \cdot \left[2\pi - \cos^{-1}\left(\frac{-A_{1k}^2 + A_{2k}^2 - A_{3k}^2}{2A_{1k}A_{3k}} \right) - \varphi_{3k} \right]. \tag{13c}$$

This solution is closely related to the law of cosines [36] and can also be derived accordingly [12]. It enables the elimination of one harmonic component of the current. In practice, the fundamental ($k = 1$), occurring at the switching frequency, is usually chosen to be eliminated.

D. Visualization for $N = 3$

An example of an asymmetric phasor diagram can be seen in Fig. 6, which shows the fundamental components ($n = 1$) for the example waveform of Fig. 5, with D and Δi as indicated in the legend, and the three phases operating with symmetric ($\theta = 120°$) phase shift. It can be observed that since the different phases are operated under asymmetric conditions, their phasor sum does not add to zero if the conventional phase-shift is employed. Figure 7 shows the same system, when the phases are instead operated with asymmetric phase shifts, as calculated in Eqs. (13a)-(13c). With the proposed phase-shift technique, complete cancellation of the fundamental ripple component can be achieved, as observed by the fact that the three phasors of Figure 7 sum to zero (i.e., they form a closed polygon), despite their different individual magnitudes.

If the difference between the magnitudes A_{nk} is too large, it is not possible to entirely balance their real and imaginary

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

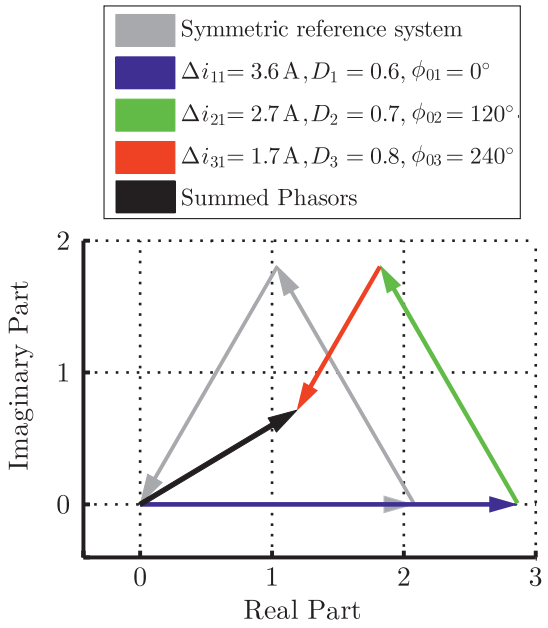


Fig. 6: Asymmetric three-phase system with symmetric phase-shift, resulting in a non-zero sum of the phasors.

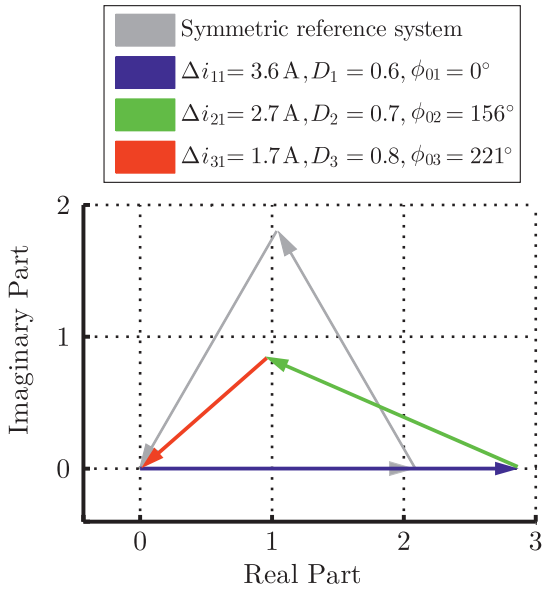


Fig. 7: Asymmetric phasor diagram with asymmetric phase-shift and symmetric reference system.

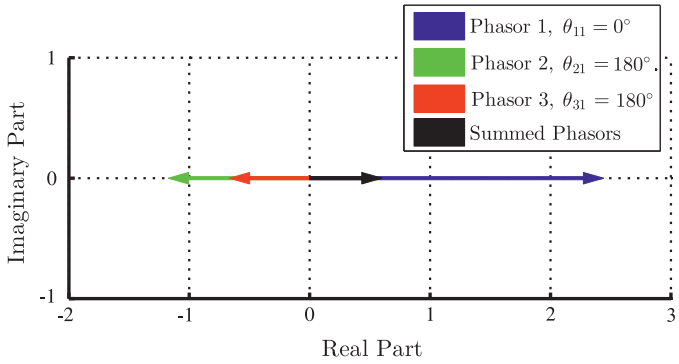


Fig. 8: Asymmetric three phase system with phase-shifts of 0° and 180° only.

parts. For $N = 3$, this corresponds to the inability to find a closed chain triangle. Consequently, a solution that minimizes a certain harmonic to zero only exists, if the magnitudes A_{nk} fulfill the triangle inequality [37]

$$||x + y|| \leq ||x|| + ||y|| \quad \forall x, y \in \{A_{1k}, A_{2k}, A_{3k}\}. \tag{14}$$

Not satisfying these conditions, results in arguments for the $\cos^{-1}$ terms with absolute values greater than one in Eqs. (13b)-(13c). Consequently, suitable angles cannot be found and the non-zero minimum of the cost function (Eq. (11)) is obtained at phase-shift angles of either 0° or 180°, as has been shown in [32]. This ensures that the expression in the cost function that corresponds to the imaginary part of the phasors is kept at zero. The real part is minimized by operating the two phases with the smaller values for A_{nk} in phase, while the phase with the highest A_{nk} is operated with a 180° phase-shift relative to the other two. This phase-shifting is illustrated in Fig. 8.

E. Solutions for $N > 3$

As shown above, it is necessary to solve $N - 1$ equations in order to determine the desired phase-shift angles. For each harmonic component, two equations occur, of which one describes the real- and one describes the imaginary-part of the corresponding phasors (see Eq. (11)). Consequently, it is possible to eliminate

$$M = \left\lfloor \frac{N-1}{2} \right\rfloor \tag{15}$$

harmonics with a given number of N phases [13]. Due to the complexity of the problem for many phases, the solution will preferably be obtained iteratively.

A minimization problem as formulated in Eq. (10) can, for example, be solved by Newton's method [38]. A vector $\Phi = [0, \phi_{02}, ..., \phi_{0N}]$ can be constructed, where the phase-shift angle ϕ_{01} is set to zero as discussed above. This vector is used as a parameter for a vector function $F(\Phi)$ of order $N-1$. The phase-shift angles can then be obtained iteratively by solving the Newton iteration sequence

$$\Phi_{k+1} = \Phi_k - F'(\Phi_k)^{-1} F(\Phi_k). \tag{16}$$

The starting values Φ_0 need to be chosen appropriately (close enough to the solution) in order to support convergence of the iteration sequence. In [13] a modified iteration method for small deviations was presented.

As shown in Eq. (17), the magnitude of the current ripple for the considered buck-converter topology is dependent on the input voltage and duty cycle.

$$\Delta i_n = \frac{V_{in,n}}{L_n} D_n (1 - D_n) \mathrm{T}. \tag{17}$$

Consequently, the derived technique can generally also be applied in regular symmetrical interleaved multiphase converters to compensate for tolerances in the inductor values L_n and slight mismatches in the operating duty ratios D_n. In case of the DMPPT application described in Section I, the input voltage $V_{in,n}$ is controlled such that it equals the voltage of the sub-module at its MPP (V_{MPP}).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

III. Control Technique for $N = 3$

Based on the results presented in Section II, a control technique can be established. For the aforementioned technique to be applicable, the value of the current ripple Δi_n has to be calculated as shown in Eq. (17) for the buck converter. Subsequently, the Fourier coefficients b_{nk}, A_{nk}, and φ_{nk} are determined as given by Eqs. (5), (6), and (7c). Therefore, the necessary parameters which have to be known in order to be able to perform the calculations are $V_{in,n}$, D_n, L_n, T, and k. $V_{in,n}$ can easily be measured, e.g., with the analog-to-digital converter (ADC) of the employed microcontroller. The value of the inductance L_n is determined by the hardware setup and is known a priori. The switching period T, which is determined by the controller switching frequency f_{sw}, and the duty cycle D_n are determined by the operating point and are accessible in the control circuit. The order k of the harmonic component to be canceled is set as desired and is readily available at the time calculations are carried out. Note that knowledge of the converter current values is not necessary in order to employ the proposed ripple-minimization technique. This simplifies the required implementation, as current measurements usually necessitate additional hardware [39]. A flowchart of the resulting algorithm is shown for $N = 3$ in Fig. 9. The inputs L_n, f_{sw}, and k, as well as the controller parameter D_n are used with the measured value of $V_{in,n}$ or $V_{out,n}$ to calculate the values of Δi_n, b_{nk}, A_{nk}, and φ_{nk} sequentially. The desired phase-shift angles are obtained using the outlined solutions (Eqs. (13a)-(13c)). The values of the arguments of the $\cos^{-1}$ functions are used as a threshold to evaluate if a complete cancellation of the desired harmonic is possible, or if A_{1k}, A_{2k}, and A_{3k} fulfill the triangle inequality (Eq. (14)), respectively. Subsequently, the values of ϕ_{01}, ϕ_{02}, and ϕ_{03} are set accordingly, and the power stage controller is adjusted.

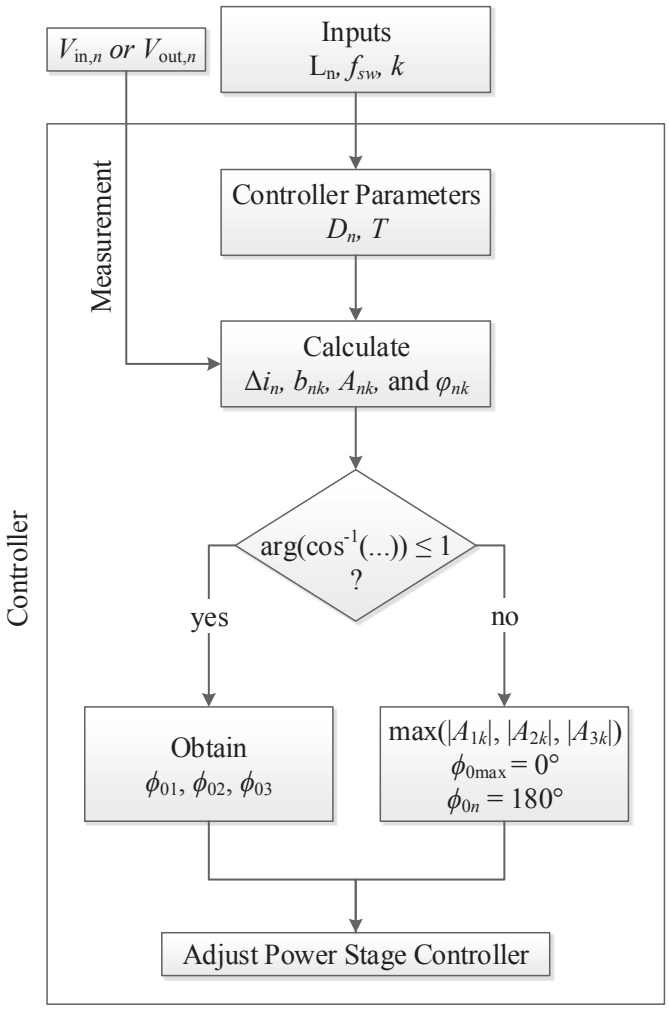


Fig. 9: Flowchart of the current ripple cancellation control.

IV. Performance Evaluation by Simulation

To evaluate the performance of the proposed ripple cancellation method, simulations in MATLAB were carried out. Additional simulation results using the circuit simulator LTspice have been presented in [30] and [32]. The three-phase buck converter topology shown in Fig. 3 is used as an example. The simulations relate to the summed inductor currents. We explore the improvement of our proposed method compared to the conventional phase-shifting technique ($\phi_{01} = 0°, \phi_{02} = 120°, \phi_{03} = 240°$) over a wide range of operating conditions. For each set of operating conditions, the converter operation was simulated with the conventional, and subsequently with the proposed, phase-shifting method applied. The relative decrease in current ripple achieved with the proposed technique has been calculated in percent as

$$\left| \frac{\Delta i_{sum} - \Delta i_{sum,sym}}{\Delta i_{sum,sym}} \right| \cdot 100\%, \tag{18}$$

where $\Delta i_{sum,sym}$ is the overall current ripple magnitude for the case with an applied symmetric phase-shift. The magnitudes A_{nk} of the corresponding phasors for a certain harmonic k are dependent on two variables per phase, namely Δi_n and D_n, which yields a six dimensional variable space for $N = 3$. We considered again the application of sub-module MPP tracking. In this case, it is possible to reduce the variable space to three dimensions by assuming that the input voltages are approximately identical for all converters. This is valid for slight variations between sub-modules, as the MPP voltages do not change substantially [11] (see Fig. 4). Moreover, the current ripple Δi_n, as given in Eq. (17), is only linearly dependent on the input voltages $V_{in,n}$, while it shows a quadratic dependency on D_n. This means that in case of a change in input voltage (e.g., due to an irradiation change of the sub-modules), the magnitude of Δi_n is scaled by a linear factor, yielding similar results. Consequently, the magnitudes of A_{nk} are approximately only dependent on the duty cycle D_n of each phase, as the current ripple is now also only dependent on this variable, if $V_{in,n}$ is fixed (see Eq. (17)). For the simulations, the input voltages have been chosen to be $V_{in,1} = V_{in,2} = V_{in,3} = 12$ V. The operating duty ratio D_n of each converter has been varied between 0.1 and 0.9 with a step size of 0.1. The calculations were carried out with the goal of minimizing the fundamental ripple component ($k = 1$). The result is a 9x9x9 matrix holding the decrease of the summed inductor current ripple in percent. However, not all values within the matrix are independent, as combinations of

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

converters running at certain duty ratios are calculated multiple times. This can be seen in Table I. It shows the results of the aforementioned simulations, where the average improvement was calculated over $D_3 = 0.1$ to 0.9, while D_1 and D_2 have been varied. By averaging over D_3, the aforementioned 9x9x9 matrix is reduced to the displayed 9x9 table. Consequently, the entries do not represent a single operating condition for D_3 but rather an average. The resulting matrix is bisymmetric, due to the previously mentioned dependency of the results. The main diagonals have been highlighted in red and blue respectively.

TABLE I: Average Improvement / % over D_3

		D_1								
		0.1	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**
D_2	**0.1**	21.7	29.6	44.1	45.6	45.1	46.9	45.6	45.6	28.6
	0.2	29.6	25.2	34.2	40.3	43.6	41.4	28.5	17.7	45.6
	0.3	44.1	34.2	27.5	37.6	38.3	33.6	16.1	28.5	45.6
	0.4	45.6	40.3	37.6	31.6	33.0	25.1	33.6	41.4	46.9
	0.5	45.1	43.6	38.3	33.0	31.2	33.0	38.3	43.6	45.1
	0.6	46.9	41.4	33.6	25.1	33.0	31.6	37.6	40.3	45.6
	0.7	45.6	28.5	16.1	33.6	38.3	37.6	27.5	34.2	44.1
	0.8	45.6	17.7	28.5	41.4	43.6	40.3	34.2	25.2	29.6
	0.9	28.6	45.6	45.6	46.9	45.1	45.6	44.1	29.6	21.7

In order to show the achievable improvement in case of one duty ratio being fixed, D_3 has been set to 0.9. High duty ratios are typical in the solar MPP tracking applications considered here, as shown in [24]. The resulting surface plot can be seen in Fig. 10. This surface can be obtained, when "slicing" the aforementioned matrix with the results at $D_3 = 0.9$. In order to achieve a better resolution, the step size has been decreased, such that D_1 and D_2 are varied between 0.1 and 0.9, with the interval now being 0.025. In the plot, we can again observe the symmetry around the red-shaded plane. The plot that can be observed when D_3 is set to 0.1 looks similar and is the mirrored image around the blue-shaded plane. Moreover, it can be observed in Fig. 10 that the achievable improvement over a conventional phase-shift is zero for $D_1 = D_3 = D_3$ as expected. Additionally, Fig. 11 shows the magnitude of the unfiltered output current ripple with an even phase-shift applied under the same operating conditions as before. As it can be observed, operating regions where a high improvement is possible coincide with operating conditions which would normally result in a high output current ripple.

V. Experimental Results

A hardware implementation of the system has been designed, consisting of three identical synchronous buck converters. Figures 12 and 13 show annotated photographs of the hardware, Table II lists the converter specifications, while Table III contains a listing of the components.

To implement the proposed control technique, all three converters are controlled by a single microcontroller (MC). This allows for precise timing of the three converters without the requirement to synchronize controllers. Moreover, control losses are reduced in comparison to an implementation with three separate MCs. The used Atmel AT90PWM316 microcontroller provides three hardware power stage controllers

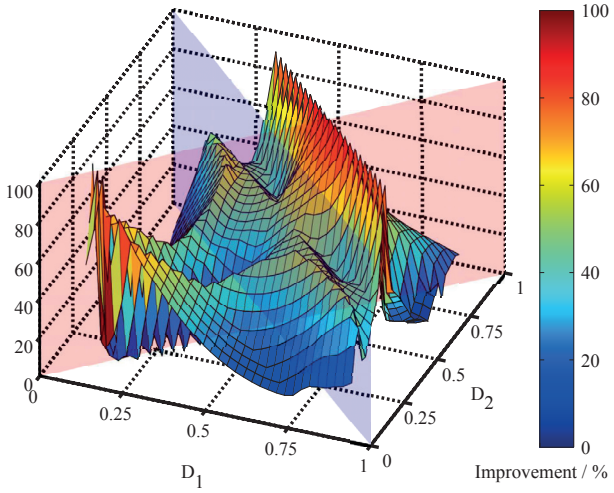


Fig. 10: Improvement in ripple cancellation for the summed inductor current with $V_1 = V_2 = V_3 = 12$ V, $D_3 = 0.9$, D_1 and D_2 varied.

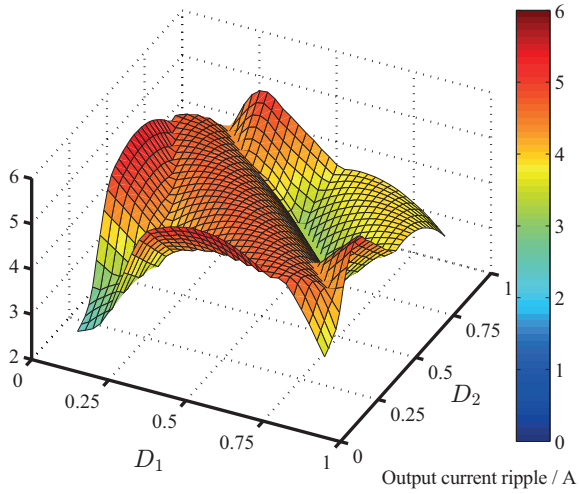
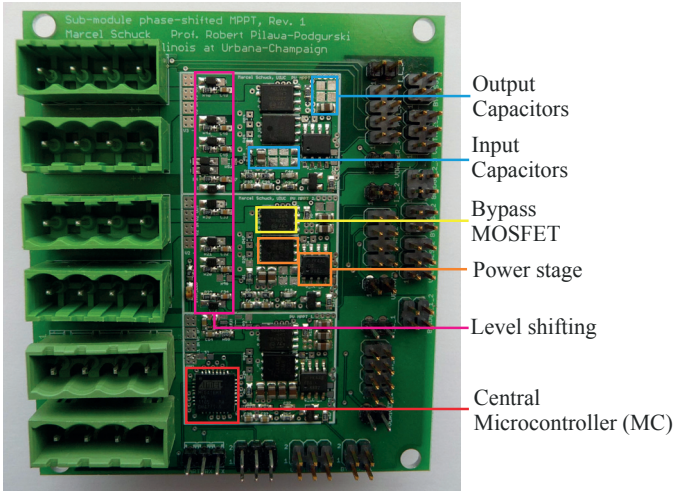


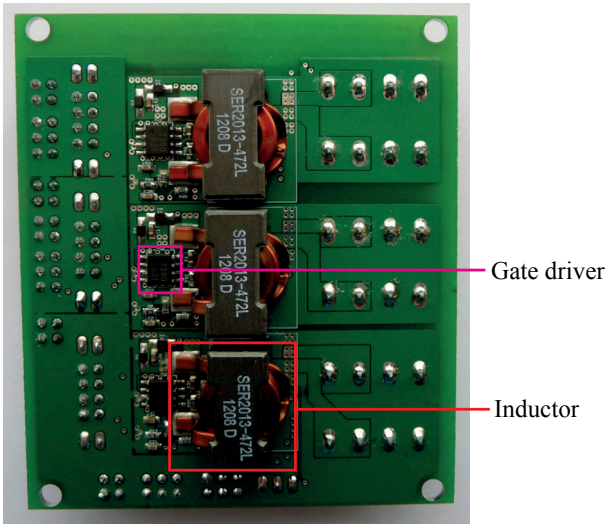
Fig. 11: Magnitude of the unfiltered output current ripple with even phase-shift applied at $V_{in,1} = V_{in,2} = V_{in,3} = 12$ V, $D_3 = 0.9$, D_1 and D_2 varied.



PCB Top Side

Fig. 12: Annotated photograph of the experimental prototype - top view of the printed circuit board (PCB).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics



PCB Bottom Side

Fig. 13: Annotated photograph of the experimental prototype - bottom view of the PCB.

TABLE II: Converter Specifications

Input Voltage Range	7 - 16 V
Output Voltage Range	1 - 14 V
Max. Output Power per Converter	100 W
Switching Frequency	100 kHz
Converter Peak Efficiency	95%
Board Area per Converter	21 mm x 27 mm
Overall Board Area	63 mm x 27 mm

TABLE III: Component Listing

Device	Model	Value	Manufacturer
High side MOSFET	FDMS8023S		Fairchild
Low side MOSFET	FDS8882		Fairchild
Gate driver	FAN7390MX		Fairchild
Bypass MOSFET	STL150N3LLH5		ST
L_n	SER2300	4.7 μH	Coilcraft
C_{INn}	1206, X5R, 16 V	4 x 10 μF	Taiyo Yuden
C_{OUTn}	1206, X5R, 16 V	3 x 10 μF	Taiyo Yuden
Microcontroller	AT90PWM316		Atmel

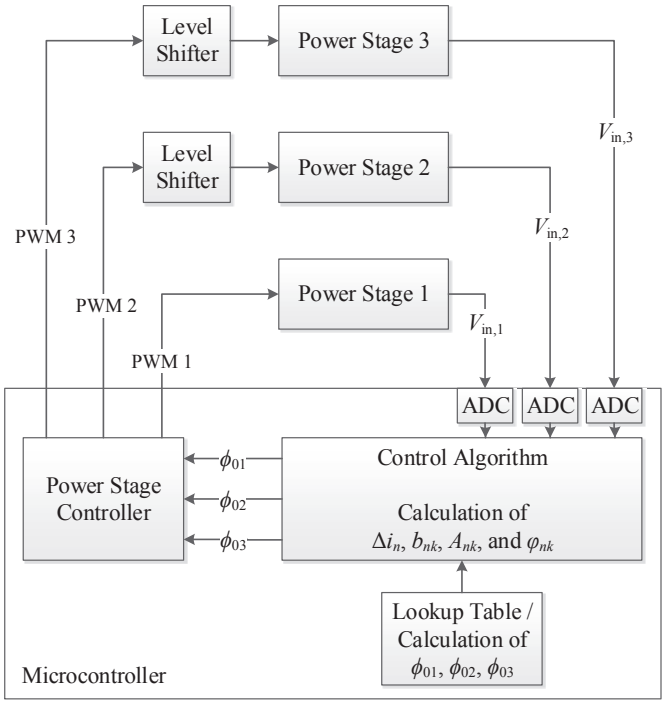


Fig. 14: Control architecture of the experimental prototype.

(PSCs) for easy interfacing with the gate drivers. An on-chip PLL with a frequency of up to 64 MHz is used for accurate PWM waveform generation. The three PSCs are initialized with the desired PWM values (duty cycles, dead times, frequency) by setting the corresponding MC registers. The phase-shift of the waveforms is implemented by starting the waveform outputs at different times. This is coordinated by events (interrupts) generated by the internal timer as shown in Fig. 15. When changed operating conditions, that require a different phase-shift for ripple minimization, have been detected, the PSCs are restarted accordingly with the new timer values. With the switching frequency of the prototype (f_{sw} = 100 kHz), these adjustments are possible during operation within one switching period. More information on the PSC, PLL and timers of the microcontroller used for the prototype can be found in [40], [41]. It should be noted, that the approach to generate the PWM waveforms, as described here, is dependent on the PWM architecture of the employed MC and might be different for other controller types. The desired asymmetric phase-shift angles can either be calculated in real-time or taken from a precalculated lookup table. During operation, the MC continuously measures the input voltage $V_{in,n}$ of each converter through its ADCs. Based on these measurements, the Δi_n values are calculated as shown by Eq. (2). This is possible, because all other required variables are known to the controller, as discussed in Section III. These values are used as an input to perform a search or interpolation of the corresponding phase-angles ϕ_{01}, ϕ_{02} and ϕ_{03} from the lookup table. The size of the lookup table can significantly be reduced by utilizing the symmetry properties of the solutions as discussed in Section IV. Alternatively, Eqs. (13a)-(13c) can be implemented in the controller for online calculation, which reduces the required storage space. However, computational requirements are increased. Reference [33] contains an analysis of the trade-off between lookup table size and computing time for a related application. The corresponding control architecture for adjusting the phase-shift of all three converters is shown in Fig. 14. In case multiple prototype modules, each consisting of three converters, are used, a synchronization between all controllers has to be implemented. However, this is only required if it is intended to use more than the three phases per module to improve ripple cancellation. In the PV application intended here, there is additional complexity of synchronization between PV modules (e.g., added wiring) if an asymmetric phase-shift beyond a single PV module is desired. In a typical scenario, we envision that ripple cancellation between three sub-modules alone (i.e., at the PV module level) provides the best trade-off between implementation

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

complexity and overall component size/cost reduction. The prototype converters can be connected differently to either implement a series-connected topology (as shown in Fig. 3) or a parallel-connected topology. Figure 16 shows the calculated phase currents for three converters at the operating conditions $V_{in,1} = 14$ V, $V_{in,2} = 12$ V, and $V_{in,3} = 10$ V and duty cycles $D_1 = 0.6$, $D_2 = 0.7$, and $D_3 = 0.8$ (see phasor diagram shown in Fig. 7). The dc component of the phase currents has been removed, as it is equal for all converters in the output-series connection considered here. The switching frequency f_{sw} is set to 100 kHz. The resulting phase-shift angles are $\phi_{01} = 0°$, $\phi_{02} = 138.4°$, and $\phi_{03} = 185.3°$. Figure 17 shows the corresponding spectrum (A_{nk} values) of the waveforms for k from 1 to 10. Moreover, Fig. 18 shows the resulting spectrum, if the A_{nk} coefficients of all phases are added with the proposed phase-shift angles applied. It can be seen that the first harmonic is completely eliminated. Figure 19 shows the phase currents as well as the load-current measured with the converters of the experimental prototype connected in series at the same operating conditions as for the calculations ($V_{in,1} = 14$ V, $V_{in,2} = 12$ V, $V_{in,3} = 10$ V, $D_1 = 0.6$, $D_2 = 0.7$, $D_3 = 0.8$, f_{sw}= 100 kHz). Laboratory power supplies have been used as sources for the different input voltages. An electronic load has been used in constant-current mode and the common output current of all converters has been set to 5 A. A symmetric phase-shift ($\phi_{01} = 0°$, $\phi_{02} = 120°$, and $\phi_{03} = 240°$) was applied first, yielding an output current ripple of 220 mA. Figure 20 shows the measurement results with the same topology and same operating conditions, but with the proposed asymmetric phase-shifting technique applied (phase-shift angles are now $\phi_{01} = 0°$, $\phi_{02} = 138.4°$, $\phi_{03} = 185.3°$), yielding an output current ripple of 60 mA. This corresponds to a relative improvement of 73% (as calculated by Eq. (18)), or correspondingly, a 3.67x reduction in current ripple. Here, we did not assume that the input voltages were equal for all converters as in the simulations shown in Section IV. This allows us to demonstrate the performance of the proposed control scheme for a general operating point. Carrying out the simulations over a wide range of duty ratios with input voltages $V_{in,1} = 14$ V, $V_{in,2} = 12$ V, and $V_{in,3} = 10$ V (as given above), yields an average improvement in ripple reduction of 43.2%.

To analyze the frequency content of the experimentally obtained output ripple waveforms, their fast Fourier transform (FFT) was calculated using the mathematical toolset of the oscilloscope. The results are shown in Fig. 21 for a symmetric phase-shift and in Fig. 22 for the proposed asymmetric phase-shifting technique. A complete elimination of the first harmonic component, as shown in the theoretical calculations, is not achieved with the experimental setup due to timing resolution constraints and circuit tolerances. However, it can be seen that the fundamental ripple component is significantly attenuated by 14.8 dB when using the proposed method. Our experimental results thus confirm the significant improvements in ripple reduction achievable through our proposed phase-shifting technique. It should be noted that the focus of the experimental verification here has been set on steady-state ripple reduction. During transient events there will necessarily

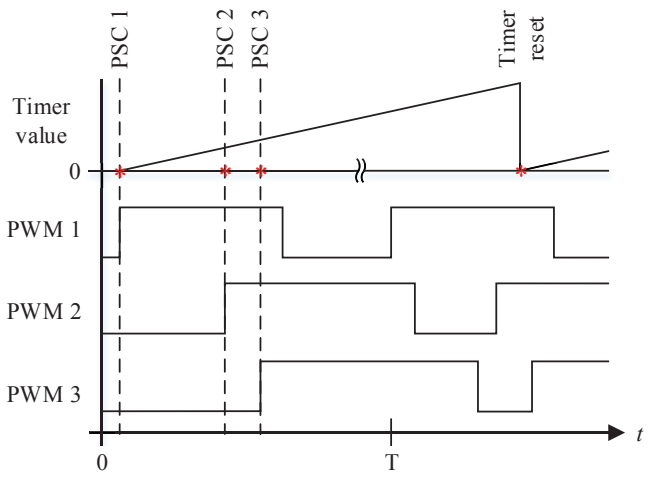


Fig. 15: Timer events for implementation of the phase-shift and corresponding PWM signals.

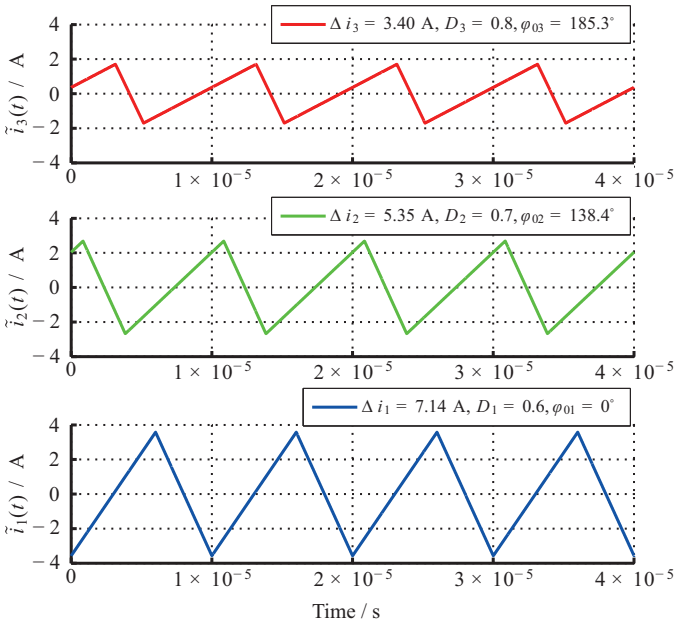


Fig. 16: Calculated ripple component of the phase currents for three converters with the proposed phase-shifting technique applied.

be a small period of time when optimum cancellation is not achieved, due to the finite time to compute and update the phase shift angles. In practice, however, solar irradiation changes in real-world applications occur at a relatively slow pace, as has been shown in the long-term field measurements of [42]. Moreover, the update interval of MPPT algorithms are typically the limiting factor in such situations, even in cases of high-speed solutions [43]–[45] making non-optimum ripple cancellation during sudden irradiation changes a relatively minor concern.

VI. Conclusions

We have presented an analytical derivation of a control strategy that enables interleaved operation and improved rip-

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

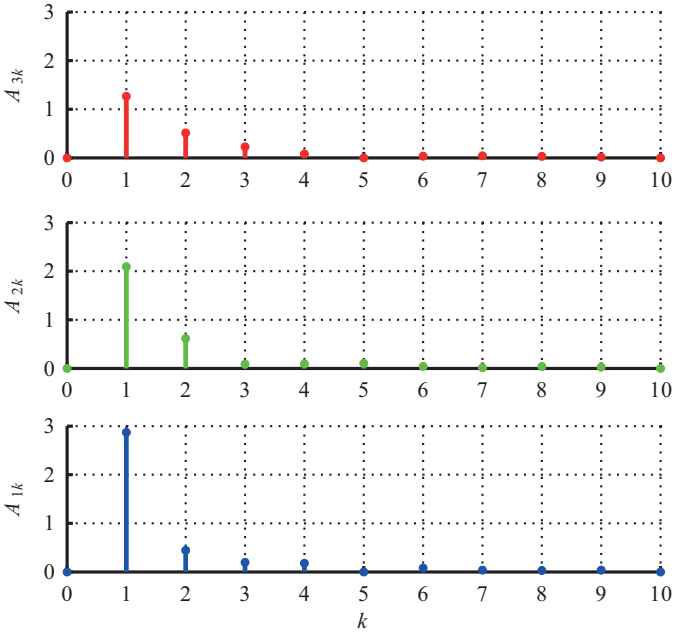


Fig. 17: Corresponding spectrum of the current ripple waveforms in each phase.

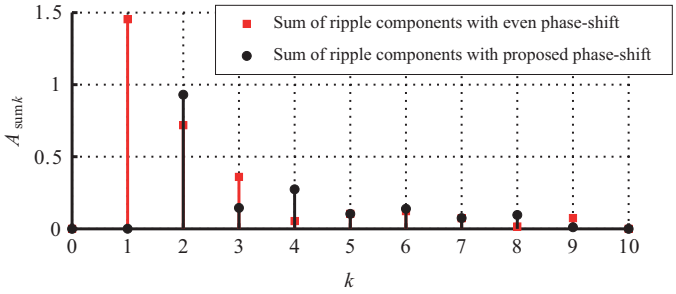


Fig. 18: Calculated spectrum for A_{nk} coefficients of all phases summed with the proposed phase-shift angles applied.

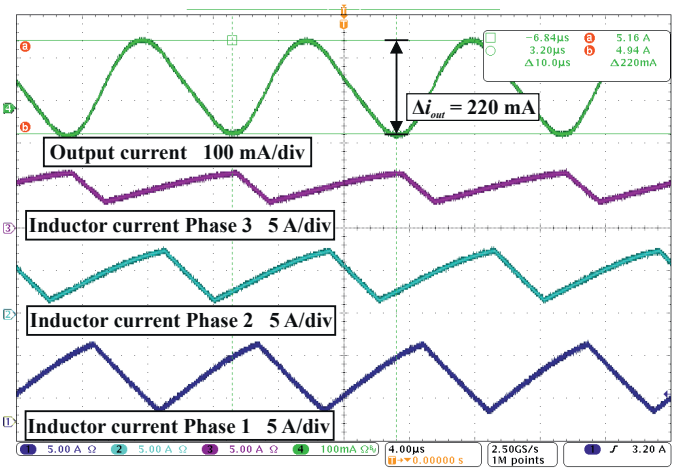


Fig. 19: Measured phase currents and load-current of the experimental prototype in series connection with symmetric phase-shift.

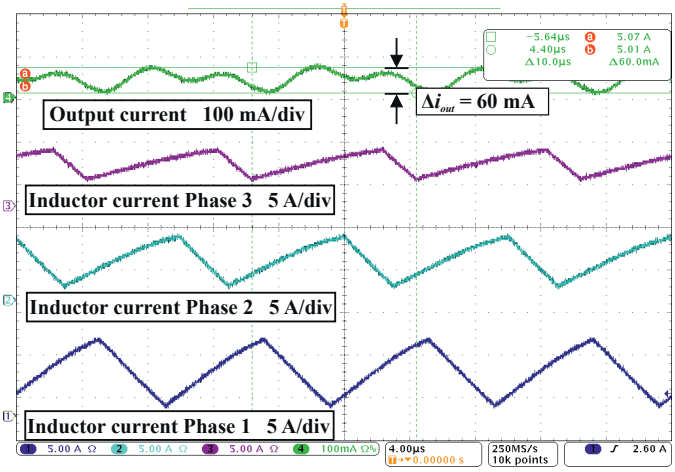


Fig. 20: Measured phase currents and load-current of the experimental prototype in series connection with proposed asymmetric phase-shift and reduced output current ripple.

ple cancellation for multiphase converters with non-uniform duty cycles. Through simulations, we have illustrated the improved performance of the proposed method compared to the conventional ripple cancellation method. The calculation of asymmetric phase-angles based on the Fourier space representation of the current ripple goes beyond the previous works in the field [34], [35], [46], [47]. Moreover, application of the proposed technique to multiphase converters with different input voltages and currents, operating at asymmetric duty cycles, extends the scope of [12]–[14] to the general case. The presented control scheme enables significant performance improvements of the converter without requiring additional hardware.

APPENDIX

A. Calculation of the Fourier coefficients

In order to represent the ripple part of the current in terms of its harmonics, the Fourier coefficients need to be obtained. To simplify the calculations, the waveform shown in Fig. 5 can be shifted such that it is point symmetric around the origin. The zero crossings now occur at 0, $T/2$, and T [36] and the resulting waveform is displayed in Fig. 23.

The time-domain representation for one period of this current waveform is given by

$$\tilde{i}(t) = \begin{cases} \dfrac{\Delta i}{DT} \cdot t & \text{for } 0 \le t \le \dfrac{DT}{2} \\ \dfrac{\Delta i}{2} - \dfrac{\Delta i}{(1-D)\frac{T}{2}} \cdot \left(t - \dfrac{DT}{2}\right) & \text{for } \dfrac{DT}{2} \le t \le T - \dfrac{DT}{2} \\ \dfrac{\Delta i}{DT} \cdot (t - T) & \text{for } T - \dfrac{DT}{2} \le t \le T. \end{cases} \tag{19}$$

Because the function is odd with zero average value,

$$a_0 = 0 \tag{20}$$

and

$$a_k = 0 \tag{21}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

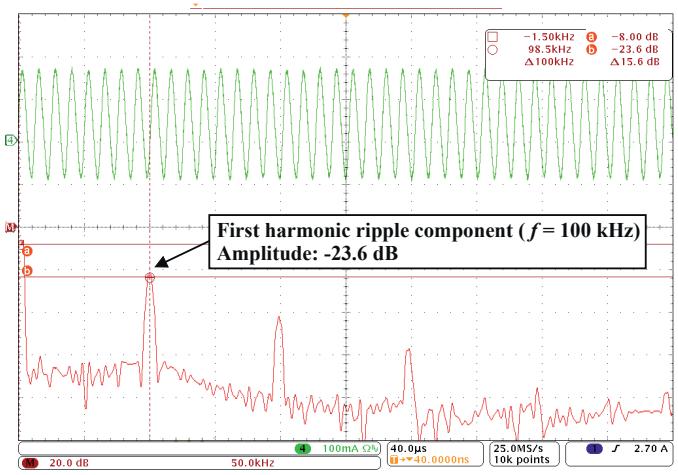


Fig. 21: Spectrum of the output current with symmetric phase-shift.

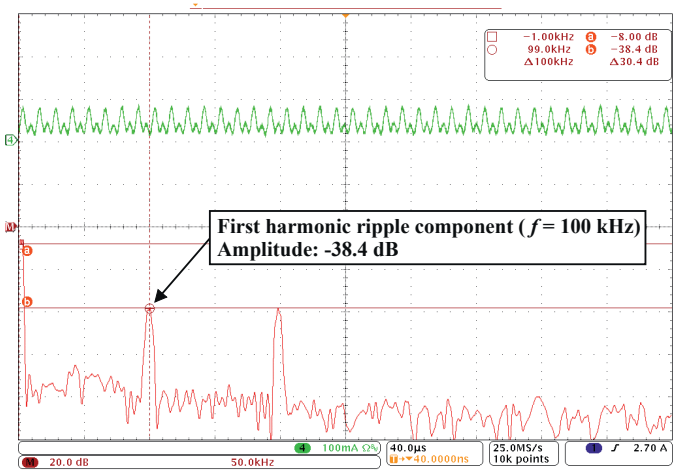


Fig. 22: Spectrum of the output current with proposed asymmetric phase-shift.

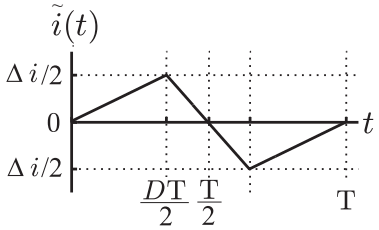


Fig. 23: Current ripple waveform for a buck converter in continuous conduction mode, time-shifted such that it is symmetrical around the origin.

holds (see [36]). The remaining coefficient b_k is calculated as:

$$b_k = \frac{2}{T}\int_0^T \tilde{i}(t)\sin(k\omega t)\,\mathrm{d}t. \tag{22}$$

Inserting the time-domain description outlined above and performing the integration yields the result

$$b_k = -\frac{\Delta i(-1)^k}{k^2 D(1-D)\pi^2}\sin\left[k(1-D)\pi\right]. \tag{23}$$

B. Derivation of the analytic solution for $N = 3$

Equation (12) can be rewritten in its cartesian form as follows:

$$\begin{aligned} &A_{1k}\cdot\cos(\theta_{1k}) - j\cdot A_{1k}\cdot\sin(\theta_{1k}) + \ldots \\ &A_{2k}\cdot\cos(\theta_{2k}) - j\cdot A_{2k}\cdot\sin(\theta_{2k}) + \ldots \\ &A_{3k}\cdot\cos(\theta_{3k}) - j\cdot A_{3k}\cdot\sin(\theta_{3k}) = 0, \end{aligned} \tag{24}$$

which yields a set of equations that can be solved for the phase angles θ_{2k} and θ_{3k} (θ_{1k} can be chosen to be zero)

$$A_{1k} + A_{2k}\cdot\cos(\theta_{2k}) + A_{3k}\cdot\cos(\theta_{3k}) = 0 \tag{25a}$$

$$A_{2k}\cdot\sin(\theta_{2k}) + A_{3k}\cdot\sin(\theta_{3k}) = 0. \tag{25b}$$

To obtain an analytic solution, Eq. (25b) is rewritten with cosine terms only, which can be be achieved by using the trigonometric identity [36]

$$\sin(x) = \begin{cases} \sqrt{1-\cos^2(x)} & \text{for } x \in [0,\pi] \\ -\sqrt{1-\cos^2(x)} & \text{for } x \in [\pi, 2\pi]\,. \end{cases} \tag{26}$$

This yields four possible variations of Eq. (25b), dependent on the values of the angles θ_{2k} and θ_{3k}:

$$\begin{aligned} &A_{2k}\cdot\sqrt{1-\cos^2(\theta_{2k})} + A_{3k}\cdot\sqrt{1-\cos^2(\theta_{3k})} = 0 \\ &\text{for} \quad \mathrm{mod}\,(\theta_{2k}, 2\pi) \in [0,\pi] \\ &\text{and} \quad \mathrm{mod}\,(\theta_{3k}, 2\pi) \in [0,\pi] \end{aligned} \tag{27a}$$

$$\begin{aligned} &A_{2k}\cdot\sqrt{1-\cos^2(\theta_{2k})} - A_{3k}\cdot\sqrt{1-\cos^2(\theta_{3k})} = 0 \\ &\text{for} \quad \mathrm{mod}\,(\theta_{2k}, 2\pi) \in [0,\pi] \\ &\text{and} \quad \mathrm{mod}\,(\theta_{3k}, 2\pi) \in [\pi,2\pi] \end{aligned} \tag{27b}$$

$$\begin{aligned} &-A_{2k}\cdot\sqrt{1-\cos^2(\theta_{2k})} + A_{3k}\cdot\sqrt{1-\cos^2(\theta_{3k})} = 0 \\ &\text{for} \quad \mathrm{mod}\,(\theta_{2k}, 2\pi) \in [\pi,2\pi] \\ &\text{and} \quad \mathrm{mod}\,(\theta_{3k}, 2\pi) \in [0,\pi] \end{aligned} \tag{27c}$$

$$\begin{aligned} &-A_{2k}\cdot\sqrt{1-\cos^2(\theta_{2k})} - A_{3k}\cdot\sqrt{1-\cos^2(\theta_{3k})} = 0 \\ &\text{for} \quad \mathrm{mod}\,(\theta_{2k}, 2\pi) \in [\pi,2\pi] \\ &\text{and} \quad \mathrm{mod}\,(\theta_{3k}, 2\pi) \in [\pi,2\pi]\,. \end{aligned} \tag{27d}$$

Due to the periodicity of the cosine function, Eq. (27a) and Eq. (27d) as well as Eq. (27b) and Eq. (27c) are linearly dependent. To achieve an imaginary part equal to zero, the first and the second term of the equation have to be of opposite sign, as the magnitudes A_{nk} are always positive. This condition leaves Eq. (27b) and Eq. (27c) as possible solutions, which are linearly dependent. Eq. (27b) was chosen to obtain the solution. The system consisting of Eq. (25a) and Eq. (25b) can now be rewritten as

$$A_{1k} + A_{2k}\cdot\cos(\theta_{2k}) + A_{3k}\cdot\cos(\theta_{3k}) = 0 \tag{28a}$$

$$A_{2k}\cdot\sqrt{1-\cos^2(\theta_{2k})} - A_{3k}\cdot\sqrt{1-\cos^2(\theta_{3k})} = 0. \tag{28b}$$

Resubstituting as shown in Eq. (8) and rearranging yields the solutions outlined in Eqs. (13a)-(13c).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

REFERENCES

[1] O. Garcia, P. Zumel, A. de Castro, and J. A. Cobos, "Effect of the tolerances in multi-phase dc-dc converters," in *Proc. IEEE 36th Power Electronics Specialists Conf. PESC '05*, 2005, pp. 1452–1457.

[2] Z. Lukic, S. M. Ahsanuzzaman, A. Prodic, and Z. Zhao, "Self-tuning sensorless digital current-mode controller with accurate current sharing for multi-phase dc-dc converters," in *Proc. Twenty-Fourth Annual IEEE Applied Power Electronics Conf. and Exposition APEC 2009*, 2009, pp. 264–268.

[3] O. Garcia, P. Zumel, A. de Castro, P. Alou, and J. A. Cobos, "Current self-balance mechanism in multiphase buck converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1600–1606, 2009.

[4] Z. Wang and H. Li, "Three-phase bidirectional dc-dc converter with enhanced current sharing capability," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 1116–1122.

[5] B. Miwa, D. Otten, and M. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual*, feb 1992, pp. 557 –568.

[6] B. A. Miwa, "Interleaved conversion techniques for high density power suplies," Ph.D. dissertation, Massachusetts Institute of Technology, June 1992.

[7] D. Perreault and J. Kassakian, "Distributed interleaving of paralleled power converters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 44, no. 8, pp. 728 –734, aug 1997.

[8] T. Kohama and T. Ninomiya, "Automatic interleaving control for paralleled converter system and its ripple estimation with simplified circuit model," in *Proc. 7th Internatonal Conf. Power Electronics ICPE '07*, 2007, pp. 238–242.

[9] R. G. Retegui, M. Benedetti, R. Petrocelli, N. Wassinger, and S. Maestri, "New modulator for multi-phase interleaved dc/dc converters," in *Proc. 13th European Conf. Power Electronics and Applications EPE '09*, 2009, pp. 1–8.

[10] S. V. Dhople, A. Davoudi, and P. L. Chapman, "Steady-state characterization of multi-phase, interleaved dc-dc converters for photovoltaic applications," in *Proc. IEEE Energy Conversion Congress and Exposition ECCE 2009*, 2009, pp. 330–336.

[11] M. Rashid, Ed., *Power Electronics Handbook, 3rd Edition*. Butterworth-Heinemann, Burlington, MA, 2011.

[12] M. L. A. Caris, H. Huisman, J. M. Schellekens, and J. L. Duarte, "Generalized harmonic elimination method for interleaved power amplifiers," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 4979–4984.

[13] M. L. A. Caris, H. Huisman, and J. L. Duarte, "Harmonic elimination by adaptive phase-shift optimization in interleaved converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 763–768.

[14] S. Waffler, J. Biela, and J. Kolar, "Output ripple reduction of an automotive multi-phase bi-directional dc-dc converter," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, sept. 2009, pp. 2184 –2190.

[15] C. Wang, M. Xu, and F. Lee, "Asymmetrical interleaving strategy for multi-channel pfc," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 1409–1415.

[16] T. Beechner and J. Sun, "Asymmetric interleaving - a new approach to operating parallel converters," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 99–105.

[17] L. Xing and J. Sun, "Motor drive system emi reduction by asymmetric interleaving," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, 2010, pp. 1–7.

[18] M. Liserre, V. G. Monopoli, A. Dell'Aquila, A. Pigazo, and V. Moreno, "Multilevel phase-shifting carrier PWM technique in case of non-equal dc-link voltages," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, 2006, pp. 1639–1642.

[19] T. L. M., J. N. Chiasson, Z. Du, and K. J. McKenzie, "Elimination of harmonics in a multilevel converter with nonequal DC sources," *IEEE Trans. Ind. Appl.*, vol. 41, no. 1, pp. 75–82, 2005.

[20] R. C. N. Pilawa-Podgurski, "Architectures and circuits for low-voltage energy conversion and applications in renewable energy and power management," Ph.D. dissertation, Department of Electrical Engineering and Computer Science Massachusetts Institute of Technology, 2012. [Online]. Available: http://dspace.mit.edu/handle/1721.1/71485

[21] S. Qin and R. C. N. Pilawa-Podgurski, "Sub-module differential power processing for photovoltaic applications," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 101–108.

[22] S. Qin, A. Morrison, and R. Pilawa-Podgurski, "Enhancing micro-inverter energy capture with sub-module differential power processing," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 621–628.

[23] S. Qin, S. Cady, A. Dominguez-Garcia, and R. Pilawa-Podgurski, "A distributed approach to maximum power point tracking for photovoltaic submodule differential power processing," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2024–2040, April 2015.

[24] R. Pilawa-Podgurski and D. Perreault, "Sub-module integrated distributed maximum power point tracking for solar photovoltaic applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2957–2967, June 2013.

[25] M. Uno and A. Kukita, "Single-switch voltage equalizer using multi-stacked buck-boost converters for partially-shaded photovoltaic modules," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2014.

[26] D. Shmilovitz and Y. Levron, "Distributed maximum power point tracking in photovoltaic systems–emerging architectures and control methods," *Automatika: Journal for Control, Measurement, Electronics, Computing and Communications*, vol. 53, no. 2, pp. 142–155, 2012.

[27] N. Femia, G. Lisi, G. Petrone, G. Spagnuolo, and M. Vitelli, "Distributed maximum power point tracking of photovoltaic arrays: Novel approach and system analysis," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2610–2621, 2008.

[28] J. Stauth, M. Seeman, and K. Kesarwani, "Resonant switched-capacitor converters for sub-module distributed photovoltaic power management," *Power Electronics, IEEE Transactions on*, vol. 28, no. 3, pp. 1189–1198, March 2013.

[29] S. Kjaer, J. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, 2005.

[30] M. Schuck and R. Pilawa-Podgurski, "Ripple minimization in asymmetric multiphase interleaved DC-dc switching converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 133–139.

[31] M. Schuck, "Implementation and control of distributed maximum power point tracking in solar photovoltaic applications," Master Thesis, Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, 2013. [Online]. Available: http://hdl.handle.net/2142/44124

[32] M. Schuck and R. C. N. Pilawa-Podgurski, "Input current ripple reduction through interleaving in single-supply multiple-output dc-dc

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2393812, IEEE Transactions on Power Electronics

converters," in *14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2013.

[33] A. Ho, M. Schuck, and R. Pilawa-Podgurski, "Asymmetric interleaving in low-voltage cmos power management with multiple supply rails," in *IEEE Energy Conversion Congress and Exposition*, 2014.

[34] B. Hu and S. Sathiakumar, "Current ripple cancellation of multiple paralleled boost converters for pv/battery charging system with mppt," in *Proc. IEEE PES Innovative Smart Grid Technologies Asia (ISGT)*, 2011, pp. 1–6.

[35] H. Boyang and S. Sathiakumar, "A novel switching technique of current ripple cancellation for multi-input sources with paralleled buck converters," in *Innovative Smart Grid Technologies Asia (ISGT), 2011 IEEE PES*, Nov. 2011, pp. 1 –8.

[36] E. W. Weisstein, *CRC Concise Encyclopedia of Mathematics, Second Edition*, 2nd ed. Chapman and Hall/CRC, 2002.

[37] S. G. Krantz, *Handbook of Complex Variables*. Springer, 1999.

[38] S. Brown and D. Smith, *Iterative Methods for Optimization*, 2nd ed. SIAM, 1999.

[39] H. Forghani-zadeh and G. Rincon-Mora, "Current-sensing techniques for dc-dc converters," in *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, vol. 2, 2002.

[40] *AT90PWM316 8-bit Microcontroller Datasheet*, Atmel Corporation, 7 2013, rev. 7710H.

[41] *AVR434:PSC Cookbook*, Atmel Corporation, 10 2006, rev. 7670A.

[42] R. Serna, B. Pierquet, J. Santiago, and R. Pilawa-Podgurski, "Field measurements of transient effects in photovoltaic panels and its importance in the design of maximum power point trackers," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 3005–3010.

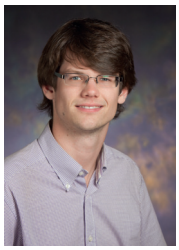
[43] A. Latham, R. Pilawa-Podgurski, K. Odame, and C. Sullivan, "Analysis and optimization of maximum power point tracking algorithms in the presence of noise," *Power Electronics, IEEE Transactions on*, vol. 28, no. 7, pp. 3479–3494, July 2013.

[44] C. Barth and R. Pilawa-Podgurski, "Implementation of dithering digital ripple correlation control for pv maximum power point tracking," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, June 2013, pp. 1–7.

[45] C. Barth and R. Pilawa-Podgurski, "Dithering digital ripple correlation control with digitally-assisted windowed sensing for solar photovoltaic mppt," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 1738–1746.

[46] S. Utz, M. Stadler, and J. Pforr, "Active phase-shift control of multiphase converters to minimize input current sub-harmonics," in *Proc. 13th European Conf. Power Electronics and Applications EPE '09*, 2009, pp. 1–10.

[47] K.-Y. Cheng, F. Yu, Y. Yan, F. C. Lee, P. Mattavelli, and W. Wu, "Analysis of multi-phase hybrid ripple-based adaptive on-time control for voltage regulator modules," in *Proc. Twenty-Seventh Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)*, 2012, pp. 1088–1095.



Marcel Schuck (S'13) received the B.Sc. degree in Electrical and Computer Engineering from the Technische Universität Darmstadt, Germany, in 2011 and the M.Sc. degree in the same field from the University of Illinois at Urbana-Champaign, in 2013. He holds an MBA degree, which he received from the Collège des Ingénieurs, Paris, France, in 2014. He is currently pursuing a Ph.D. degree at the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland. His research focus is on small size, high efficiency dc-dc converters for solar photovoltaic applications and on ultra-high speed bearingless drive systems.

Robert Pilawa-Podgurski (S'06, M'11) was born in Hedemora, Sweden. He received dual B.S. degrees in physics, electrical engineering and computer science in 2005, the M.Eng. degree in electrical engineering and computer science in 2007, and the Ph.D. degree in electrical engineering in 2012, all from the Massachusetts Institute of Technology.

He is currently an Assistant Professor in the Electrical and Computer Engineering Department at the University of Illinois, Urbana-Champaign, and is affiliated with the Power and Energy Systems group. He performs research in the area of power electronics. His research interests include renewable energy applications, energy harvesting, CMOS power management, and advanced control of power converters. Dr. Pilawa-Podgurski received the Chorafas Award for outstanding MIT EECS Master's thesis, the Google Faculty Research Award, and the Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society. He is co-author of three IEEE prize papers.