In The Name Of God

Power Electronics

Power Transistors

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Out Line

The aims of this chapter are:

- To learn the characteristics of an ideal switch
- To learn about different power transistors such as BJTs, MOSFETs, SITs, IGBTs, and COOLMOS.
- To learn the limitations of transistors as switches
- To understand the characteristics, gate control requirements, and models of power transistors

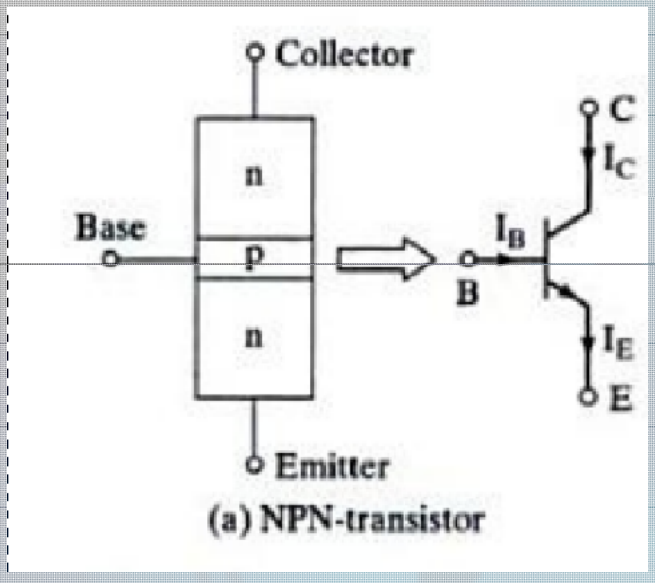
Introduction

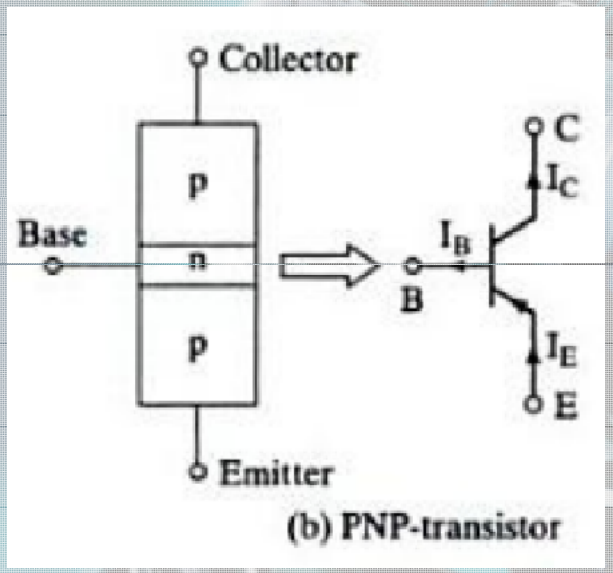
Power transistors have controlled turn-on and turn-off characteristics. The transistors, which are used as switching elements, are operated in the saturation region, resulting in a low on-state voltage drop. The switching speed of modern transistors is much higher than that of thyristors and they are extensively employed in dc–dc and dc–ac converters, with inverse parallel-connected diodes to provide bidirectional current flow. However, their voltage and current ratings are lower than those of thyristors and transistors are normally used in low- to medium-power applications. The power transistors can be classified broadly into five categories:

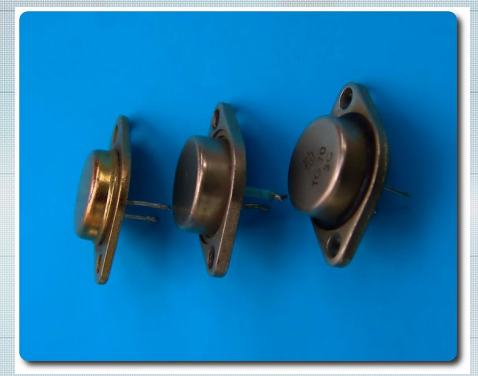
1. Bipolar junction transistors (BJTs)
2. Metal oxide semiconductor field-effect transistors (MOSFETs)
3. Static induction transistors (SITs)
4. Insulated-gate bipolar transistors (IGBTs)
5. COOLMOS

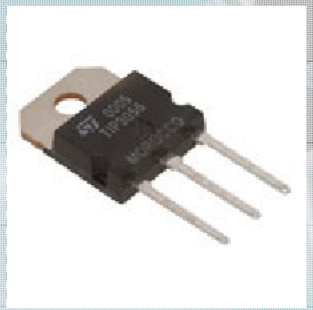
Bipolar Junction Transistors (BJT)

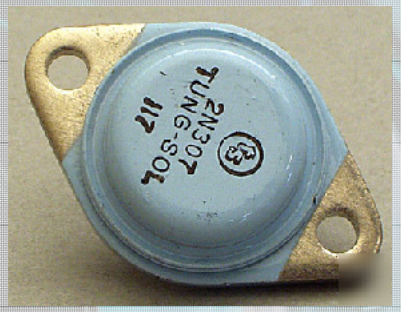
A bipolar transistor is formed by adding a second *p*- or *n*-region to a *pn*-junction diode.





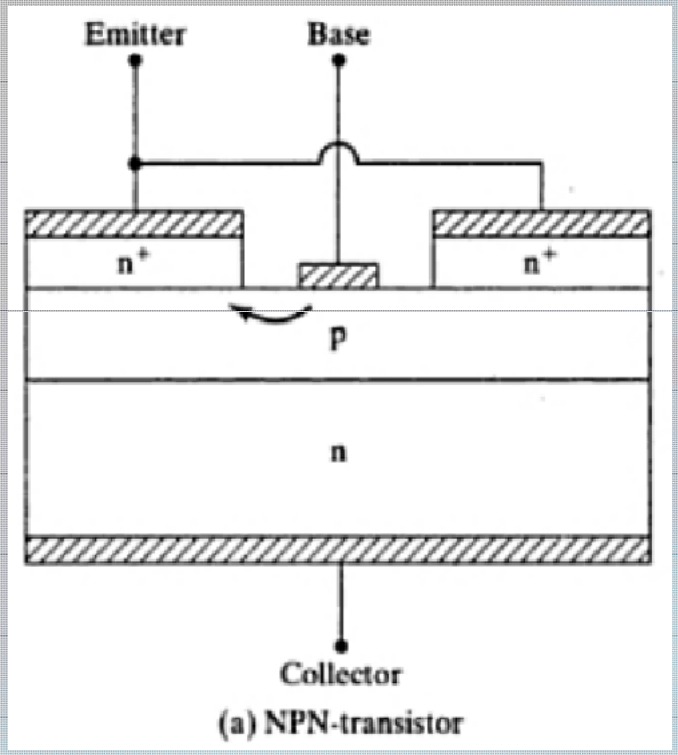






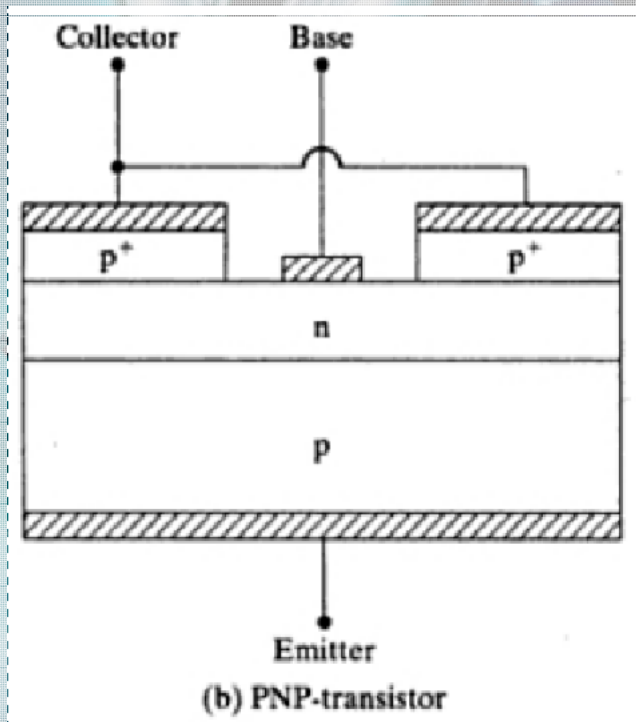
A bipolar transistor has two junctions, collector–base junc tion (CBJ) and base–emitter junction (BEJ)

There are two n^+-regions for the emitter of *NPN*-type transistor



(a) NPN-transistor

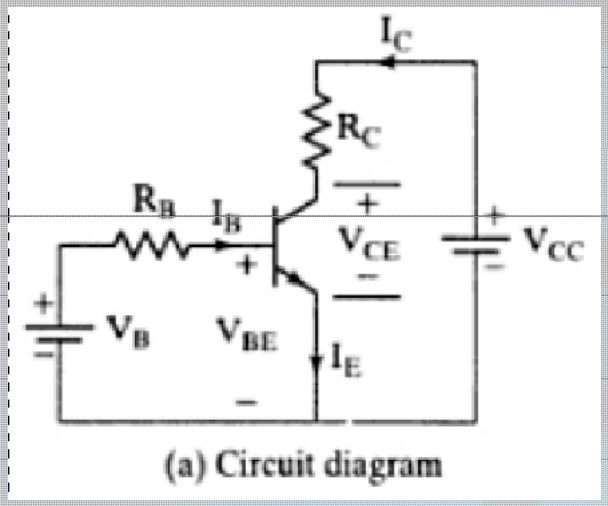
two p^+-regions for the emitter of the *PNP*-type transistor



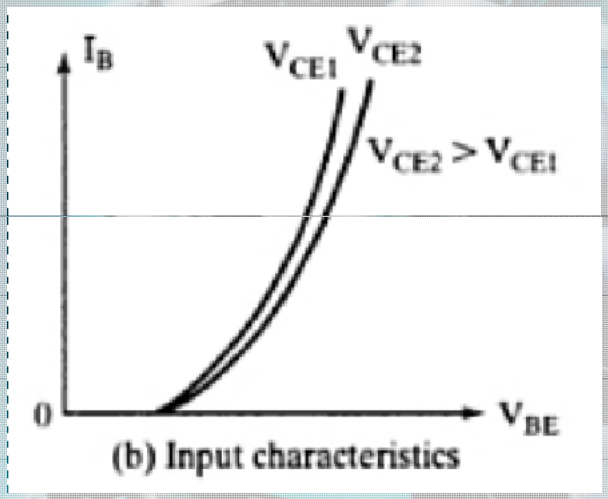
(b) PNP-transistor

Steady State Characteristics

Although there are three possible configurations—common collector, common base, and common emitter, the common-emitter configuration for an *NPN*-transistor, is generally used in switching applications.

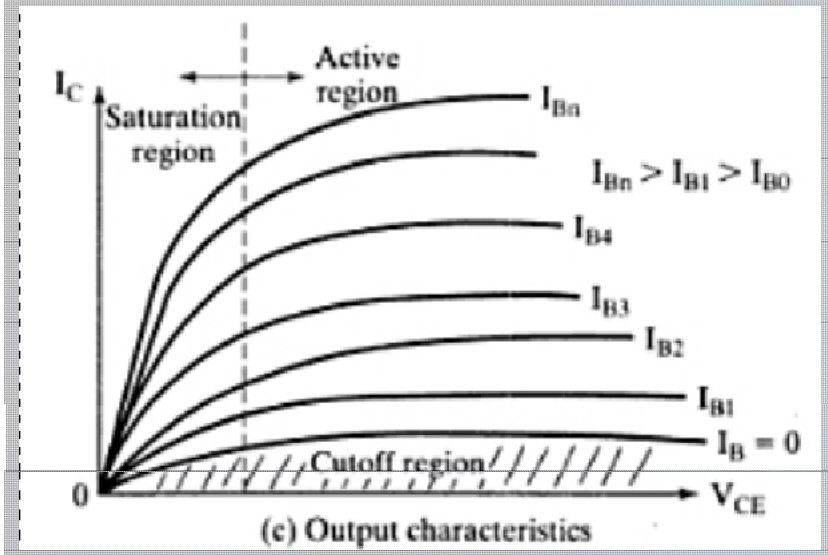


(a) Circuit diagram

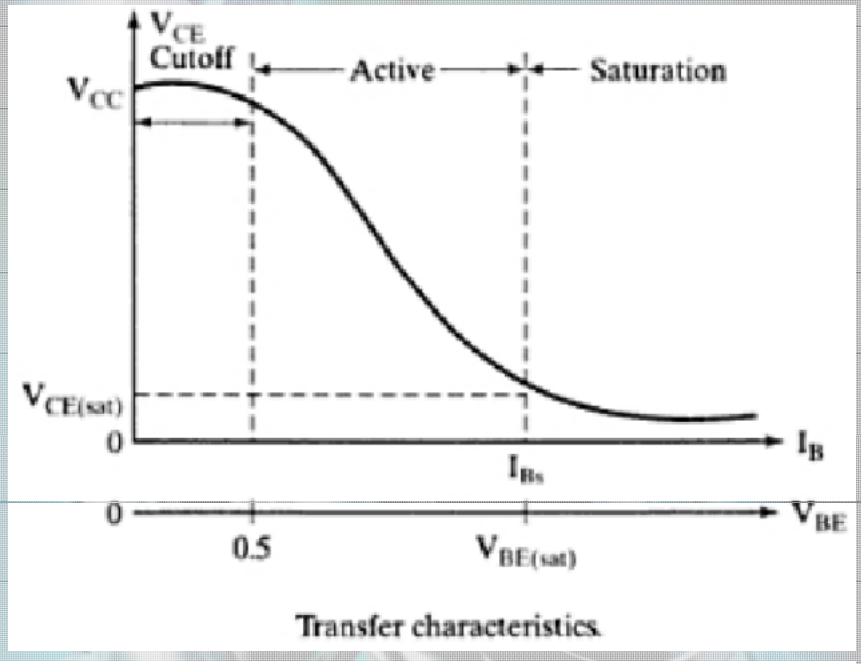


(b) Input characteristics

Output Characteristics



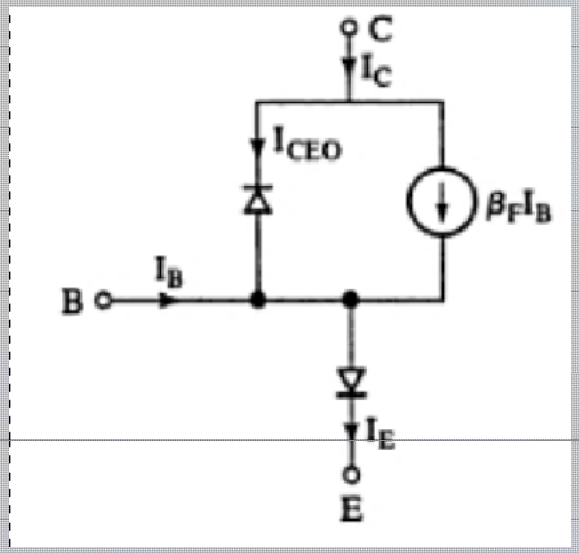
(c) Output characteristics



Transfer characteristics

the cutoff region, the transistor is off or the base current is not enough to turn it on and both junctions are reverse biased. In the active region, the transistor acts as an amplifier, where the base current is amplified by a gain and the collector–emitter voltage decreases with the base current. The CBJ is reverse biased, and the BEJ is forward biased. In the saturation region, the base current is sufficiently high so that the collector–emitter voltage is low, and the transistor acts as a switch. Both junctions (CBJ and BEJ) are forward biased.

The Model of an NPN-Transistors under Large-signal DC Operation



$$I_E = I_C + I_B$$

The base current is effectively the input current and the collector current is the output current. The ratio of the collector current I_C, to base current I_B, is known as the forward *current gain*, β_F:

$$\beta_F = h_{FE} = \frac{I_C}{I_B}$$

The collector current has two components: one due to the base current and the other is the leakage current of the CBJ.

$$I_C = \beta_F I_B + I_{CEO}$$

where I_{CEO} is the collector-to-emitter leakage current with base open circuit and can be considered negligible compared to $\beta_F I_B$.

$$I_E = I_C + I_B$$

$$I_E = I_B(1 + \beta_F) + I_{CEO}$$

$$\approx I_B(1 + \beta_F)$$

$$I_E \approx I_C\left(1 + \frac{1}{\beta_F}\right) = I_C\frac{\beta_F + 1}{\beta_F}$$

Because $\beta_F \gg 1$, the collector current can be expressed as

$$I_C \approx \alpha_F I_E$$

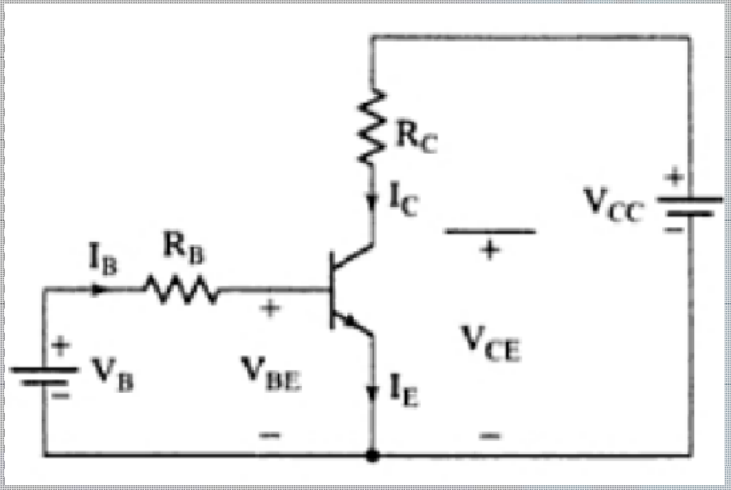
where the constant α_F is related to β by

$$\alpha_F = \frac{\beta_F}{\beta_F + 1}$$

or

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

Transistor as a Switch



$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C = V_{CC} - \frac{\beta_F R_C}{R_B}(V_B - V_{BE})$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE}$$

indicates that as long as $V_{CE} \geq V_{BE}$, the CBJ is reverse biased and the transistor is in the active region. The maximum collector current in the active region, which can be obtained by setting $V_{CB} = 0$ and $V_{BE} = V_{CE}$, is

$$I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE}}{R_C}$$

and the corresponding value of base current

$$I_{BM} = \frac{I_{CM}}{\beta_F}$$

If the base current is increased above I_{BM}, V_{BE} increases, the collector current increases, and the V_{CE} falls below V_{BE}. This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5 V. The transistor then goes into saturation. The *transistor saturation* may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In the saturation, the collector current remains almost constant. If the collector–emitter saturation voltage is $V_{CE(sat)}$, the collector current is

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

and the corresponding value of base current is

$$I_{BS} = \frac{I_{CS}}{\beta_F}$$

Normally, the circuit is designed so that I_B is higher than I_{BS}. The ratio of I_B to I_{BS} is called the *overdrive factor* (ODF):

$$\text{ODF} = \frac{I_B}{I_{BS}}$$

and the ratio of I_{CS} to I_B is called as *forced* β, β_{forced} where

$$\beta_{forced} = \frac{I_{CS}}{I_B}$$

The total power loss in the two junctions is

$$P_T = V_{BE}I_B + V_{CE}I_C$$

A high value of ODF cannot reduce the collector–emitter voltage significantly. However, V_{BE} increases due to increased base current, resulting in increased power loss in the BEJ.

Example

Finding the Saturation Parameters of a BJT

The bipolar transistor in Figure is specified to have β_F in the range of 8 to 40. The load resistance is $R_C = 11\ \Omega$. The dc supply voltage is $V_{CC} = 200$ V and the input voltage to the base circuit is $V_B = 10$ V. If $V_{CE(sat)} = 1.0$ V and $V_{BE(sat)} = 1.5$ V, find (a) the value of R_B that results in saturation with an ODF of 5, (b) the β_{forced}, and (c) the power loss P_T in the transistor.

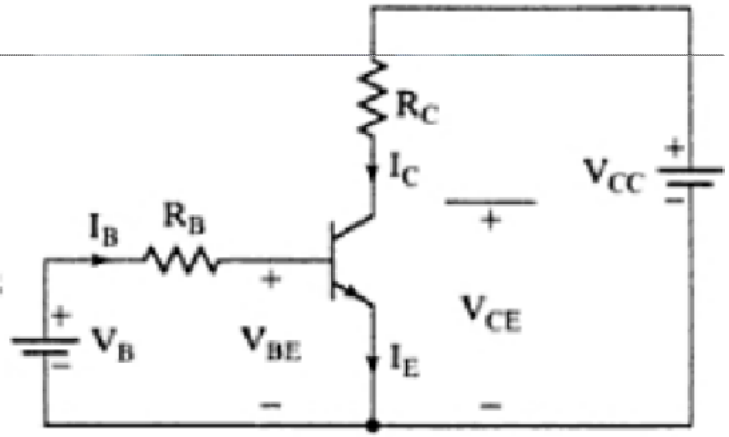
Solution

$V_{CC} = 200$ V, $\beta_{min} = 8$, $\beta_{max} = 40$, $R_C = 11\ \Omega$, ODF = 5, $V_B = 10$ V, $V_{CE(sat)} = 1.0$ V, and $V_{BE(sat)} = 1.5$ V. $I_{CS} = (200 - 1.0)/11 = 18.1$ A. $I_{BS} = 18.1/\beta_{min} = 18.1/8 = 2.2625$ A. gives the base current for an overdrive factor of 5,

$$I_B = 5 \times 2.2625 = 11.3125 \text{ A}$$

a.

$$R_B = \frac{V_B - V_{BE\,(sat)}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.7514\ \Omega$$



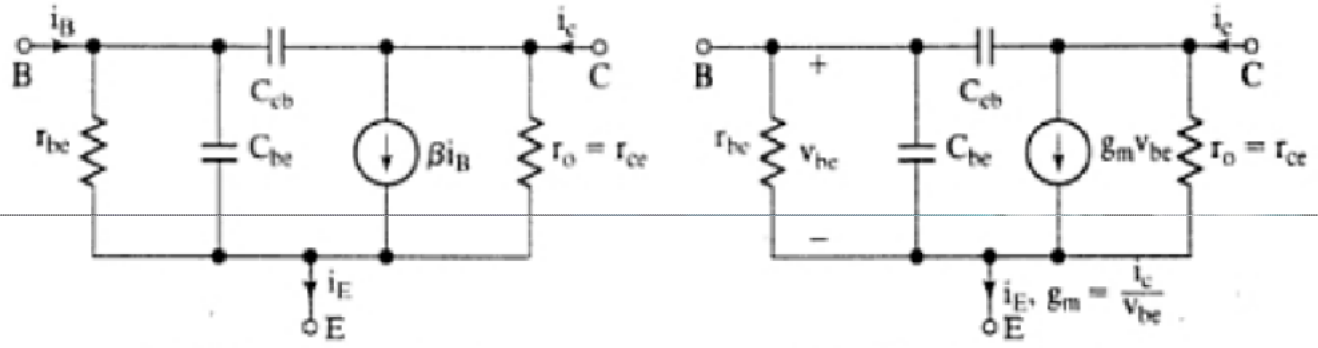
b. $\beta_{forced} = 18.1/11.3125 = 1.6.$

c.

Note: For an ODF of 10, $I_B = 22.265$ A and the power loss is $P_T = 1.5 \times 22.265 + 18.1 = 51.5$ W. Once the transistor is saturated, the collector–emitter voltage is not reduced in relation to the increase in base current. However, the power loss is increased. At a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand, if the transistor is underdriven ($I_B < I_{CB}$), it may operate in the active region and V_{CE} increases, resulting in increased power loss.

Switching Characteristics

A forward-biased *pn*-junction exhibits two parallel capacitances: a depletion-layer capacitance and a diffusion capacitance. On the other hand, a reverse-biased *pn*-junction has only depletion capacitance. Under steady-state conditions, these capacitances do not play any role. However, under transient conditions, they influence the turn-on and turn-off behavior of the transistor.

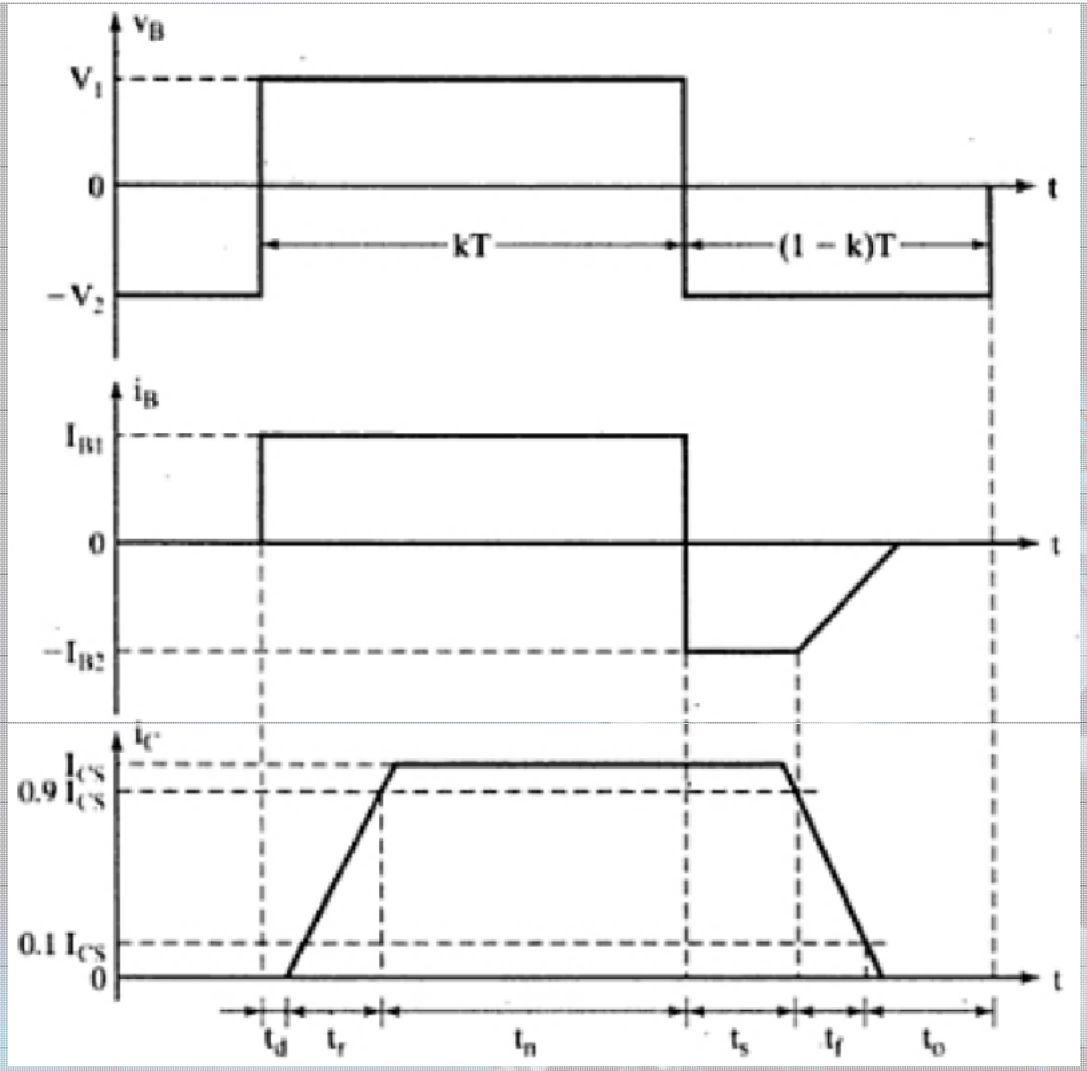


(a) Model with current gain (b) Model with transconductance

Transient model of BJT.

C_{cb} and C_{be} are the effective capacitances of the CBJ and BEJ.

The *transconductance*, g_m, of a BJT is defined as the ratio of ΔI_C to ΔV_{BE}.



Due to internal capacitances, the transistor does not turn on instantly.

delay time, t_d

delay is required to charge up the capacitance of the BEJ to the forward-bias voltage V_{BE} (approximately 0.7 V)

The rise time t_r depends on the time constant determined by BEJ capacitance.

The base current is normally more than that required to saturate the transistor. As a result, the excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge, which is called the *saturating charge*, is proportional to the excess base drive and the corresponding current I_e:

$$I_e = I_B - \frac{I_{CS}}{\beta} = \text{ODF} \cdot I_{BS} - I_{BS} = I_{BS}(\text{ODF} - 1)$$

and the saturating charge is given by

$$Q_s = \tau_s I_e = \tau_s I_{BS}(\text{ODF} - 1)$$

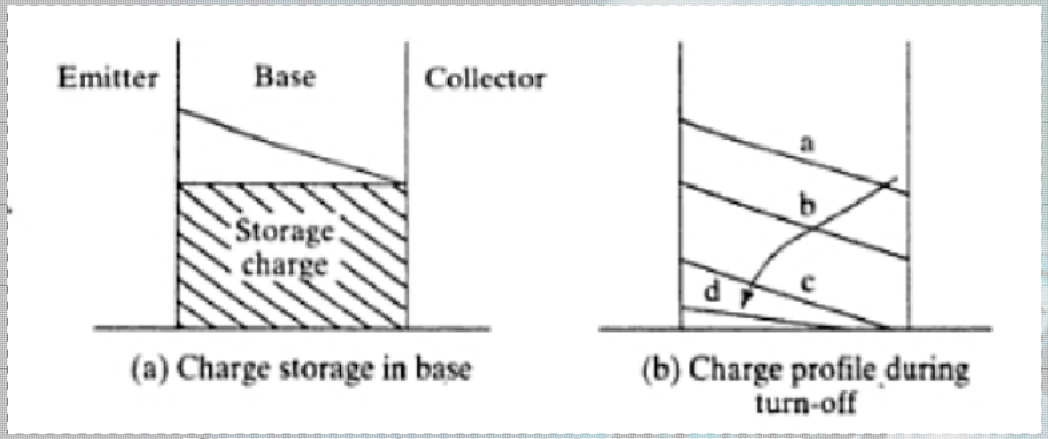
where τ_s is known as the *storage time constant* of the transistor.

When the input voltage is reversed from V_1 to $-V_2$ and the base current is also changed to $-I_{B2}$, the collector current does not change for a time t_s, called the *storage time*. The t_s is required to remove the saturating charge from the base. Because v_{BE} is still positive with approximately 0.7 V only, the base current reverses its direction due to the change in the polarity of v_B from V_1 to $-V_2$. The reverse current, $-I_{B2}$, helps to discharge the base and remove the extra charge from the base. Without $-I_{B2}$, the saturating charge has to be removed entirely by recombination and the storage time would be longer.

Once the extra charge is removed, the BEJ capacitance charges to the input voltage $-V_2$, and the base current falls to zero. The fall time t_f depends on the time constant, which is determined by the capacitance of the reverse-biased BEJ.

During turn-off, this extra charge is removed first in time t_s and the charge profile is changed from *a* to *c*

During fall time, the charge profile decreases from profile *c* until all charges are removed.



Charge storage in saturated bipolar transistors.

The turn-on time t_{on} is the sum of delay time t_d and rise time t_r:

$$t_{on} = t_d + t_r$$

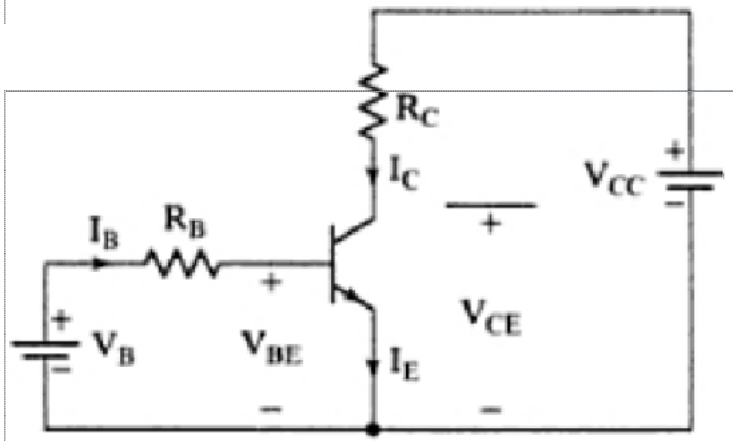
and the turn-off time t_{off} is the sum of storage time t_s and fall time t_f:

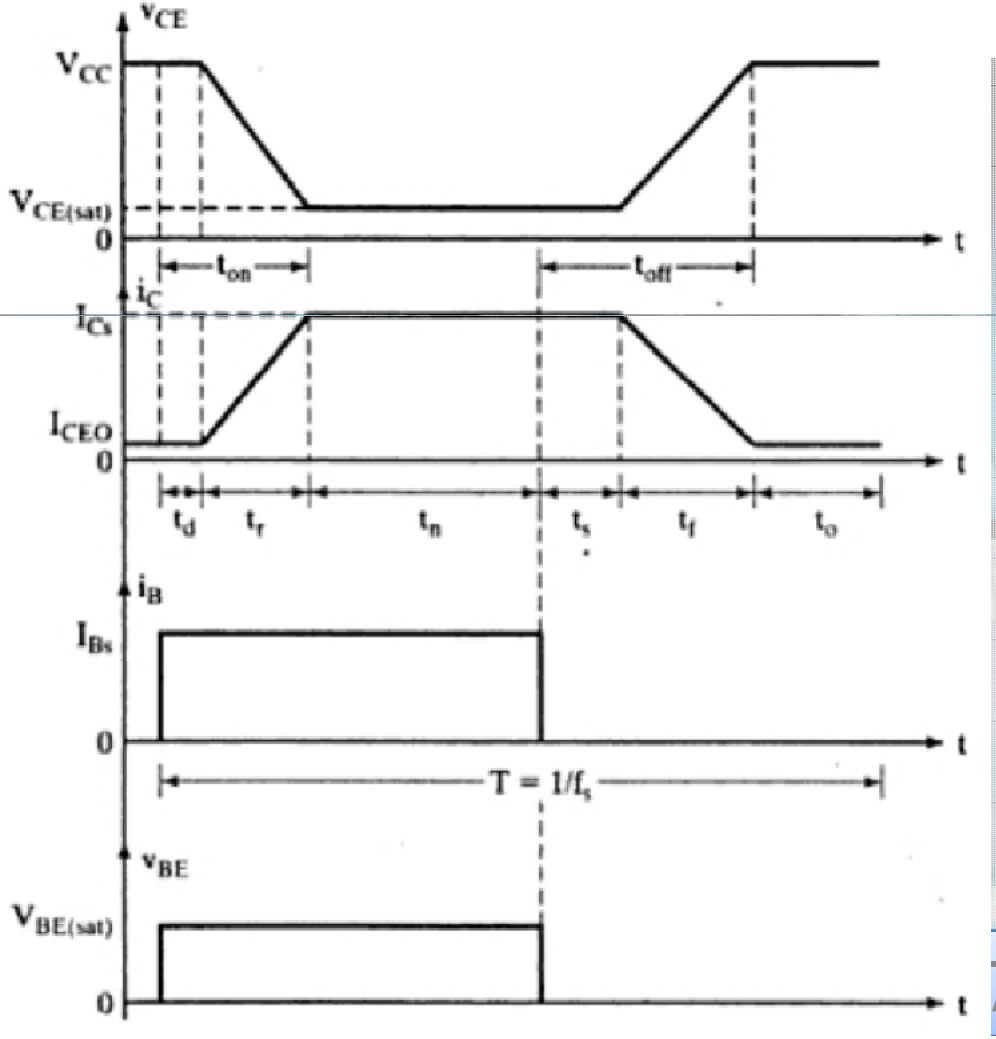
$$t_{off} = t_s + t_f$$

Example

Finding the Switching Loss of a BJT

The waveforms of the transistor switch in Figure · are shown in Figure · . The parameters are $V_{CC} = 250$ V, $V_{BE(sat)} = 3$ V, $I_B = 8$ A, $V_{CS(sat)} = 2$ V, $I_{CS} = 100$ A, $t_d = 0.5$ μs, $t_r = 1$ μs, $t_s = 5$ μs, $t_f = 3$ μs, and $f_s = 10$ kHz. The duty cycle is $k = 50\%$. The collector-to-emitter leakage current is $I_{CEO} = 3$ mA. Determine the power loss due to collector current (a) during turn-on $t_{on} = t_d + t_r$, (b) during conduction period t_n, (c) during turn-off $t_{off} = t_s + t_f$, (d) during off-time t_o, and (e) total average power losses P_T. (f) Plot the instantaneous power due to collector current $P_c(t)$.





Waveforms of transistor sw

Solution

$T = 1/f_s = 100\,\mu s$, $k = 0.5$, $kT = t_d + t_r + t_n = 50\,\mu s$, $t_n = 50 - 0.5 - 1 = 48.5\,\mu s$, $(1 - k)T = t_s + t_f + t_o = 50\,\mu s$, and $t_o = 50 - 5 - 3 = 42\,\mu s$.

a. During delay time, $0 \le t \le t_d$:

$$i_c(t) = I_{CEO}$$
$$v_{CE}(t) = V_{CC}$$

The instantaneous power due to the collector current is

$$P_c(t) = i_c v_{CE} = I_{CEO} V_{CC}$$
$$= 3 \times 10^{-3} \times 250 = 0.75\ \text{W}$$

The average power loss during the delay time is

$$P_d = \frac{1}{T}\int_0^{t_d} P_c(t)dt = I_{CEO} V_{CC} t_d f_s$$
$$= 3 \times 10^{-3} \times 250 \times 0.5 \times 10^{-6} \times 10 \times 10^3 = 3.75\ \text{mW}$$

During rise time, $0 \le t \le t_r$:

$$i_c(t) = \frac{I_{CS}}{t_r} t$$
$$v_{CE}(t) = V_{CC} + (V_{CE(sat)} - V_{CC})\frac{t}{t_r}$$

$$P_c(t) = i_c v_{CE} = I_{CS}\frac{t}{t_r}\left[V_{CC} + (V_{CE\,(sat)} - V_{CC})\frac{t}{t_r}\right]$$

The power $P_c(t)$ is maximum when $t = t_m$, where

$$t_m = \frac{t_r V_{CC}}{2[V_{CC} - V_{CE\,(sat)}]}$$

$$= 1 \times \frac{250}{2(250 - 2)} = 0.504\ \mu s$$

and

$$P_p = \frac{V_{CC}^2 I_{CS}}{4[V_{CC} - V_{CE(sat)}]}$$

$$= 250^2 \times \frac{100}{4(250 - 2)} = 6300\ W$$

$$P_r = \frac{1}{T}\int_0^{t_r} P_c(t)dt = f_s I_{CS} t_r \left[\frac{V_{CC}}{2} + \frac{V_{CE(sat)} - V_{CC}}{3}\right]$$

$$= 10 \times 10^3 \times 100 \times 1 \times 10^{-6}\left[\frac{250}{2} + \frac{2 - 250}{3}\right] = 42.33\ W$$

The total power loss during the turn-on is

$$P_{on} = P_d + P_r$$

$$= 0.00375 + 42.33 = 42.33\ W$$

b. The conduction period, $0 \le t \le t_n$:

$$i_c(t) = I_{CS}$$

$$v_{CE}(t) = V_{CE(\text{sat})}$$

$$P_c(t) = i_c v_{CE} = V_{CE(\text{sat})} I_{CS}$$

$$= 2 \times 100 = 200 \text{ W}$$

$$P_n = \frac{1}{T}\int_0^{t_n} P_c(t)dt = V_{CE(\text{sat})} I_{CS} t_n f_s$$

$$= 2 \times 100 \times 48.5 \times 10^{-6} \times 10 \times 10^3 = 97 \text{ W}$$

c. The storage period, $0 \le t \le t_s$:

$$i_c(t) = I_{CS}$$
$$v_{CE}(t) = V_{CE(sat)}$$
$$P_c(t) = i_c v_{CE} = V_{CE(sat)} I_{CS}$$
$$= 2 \times 100 = 200 \text{ W}$$
$$P_s = \frac{1}{T}\int_0^{t_s} P_c(t)dt = V_{CE(sat)} I_{CS} t_s f_s$$
$$= 2 \times 100 \times 5 \times 10^{-6} \times 10 \times 10^3 = 10 \text{ W}$$

The fall time, $0 \le t \le t_f$:

$$i_c(t) = I_{CS}\left(1 - \frac{t}{t_f}\right), \text{ neglecting } I_{CEO}$$
$$v_{CE}(t) = \frac{V_{CC}}{t_f} t, \text{ neglecting } I_{CEO}$$
$$P_c(t) = i_c v_{CE} = V_{CC} I_{CS}\left[\left(1 - \frac{t}{t_f}\right)\frac{t}{t_f}\right]$$

This power loss during fall time is maximum when $t = t_f/2 = 1.5$ µs gives the peak power,

$$P_m = \frac{V_{CC} I_{CS}}{4} = 2$$

$$P_f = \frac{1}{T}\int_0^{t_f} P_c(t)dt = \frac{V_{CC} I_{CS} t_f f_s}{6}$$
$$= \frac{250 \times 100 \times 3 \times 10^{-6} \times 10 \times 10^3}{6} = 125 \text{ W}$$

The power loss during turn-off is

$$P_{off} = P_s + P_f = I_{CS} f_s\left(t_s V_{CE(sat)} + \frac{V_{CC} t_f}{6}\right)$$
$$= 10 + 125 = 135 \text{ W}$$

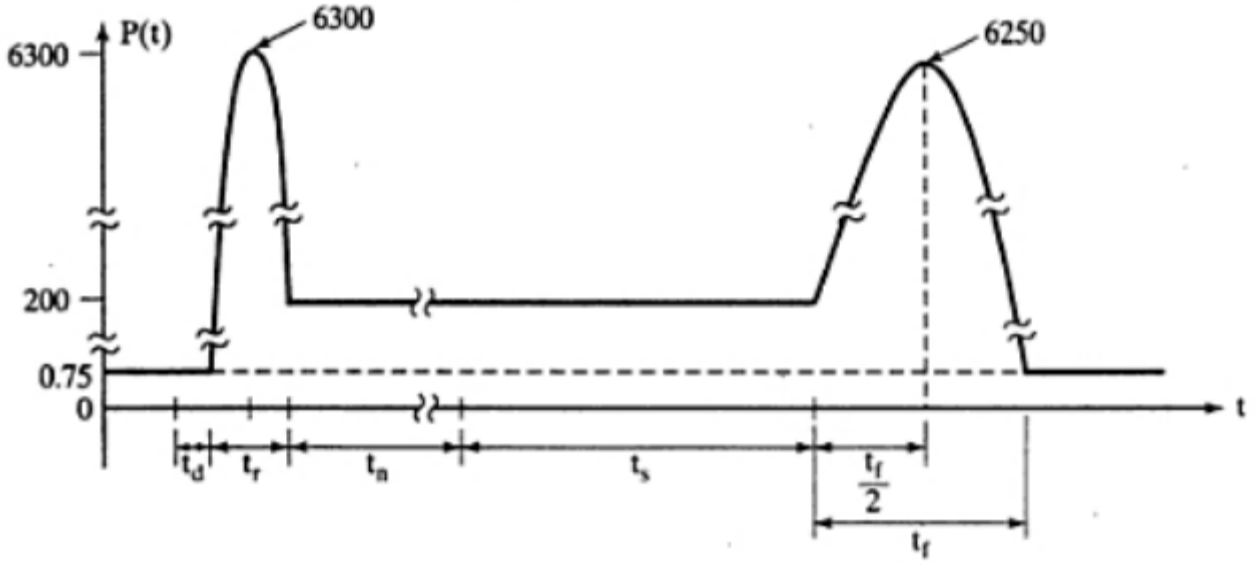
d. Off-period, $0 \le t \le t_o$:

$$i_c(t) = I_{CEO}$$
$$v_{CE}(t) = V_{CC}$$
$$P_c(t) = i_c v_{CE} = I_{CEO} V_{CC}$$
$$= 3 \times 10^{-3} \times 250 = 0.75 \text{ W}$$
$$P_0 = \frac{1}{T}\int_0^{t_o} P_c(t)dt = I_{CEO} V_{CC} t_o f_s$$
$$= 3 \times 10^{-3} \times 250 \times 42 \times 10^{-6} \times 10 \times 10^3 = 0.315 \text{ W}$$

e. The total power loss in the transistor due to collector current is

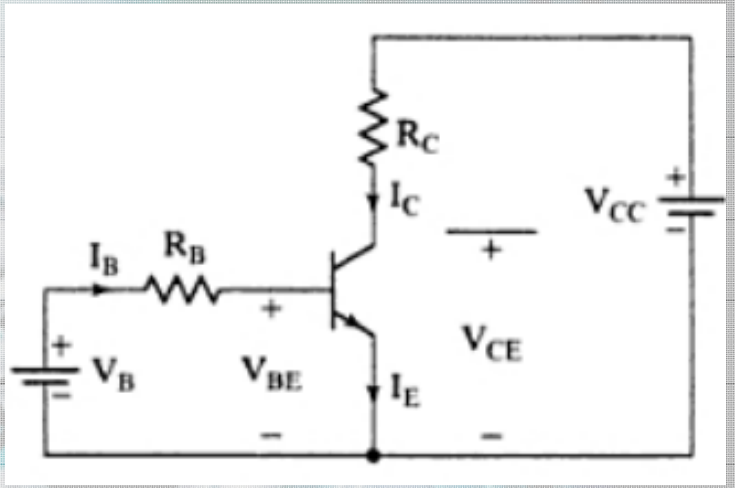
$$P_T = P_{on} + P_n + P_{off} + P_0$$
$$= 42.33 + 97 + 135 + 0.315 = 274.65 \text{ W}$$

f. The plot of the instantaneous power



Example

Finding the Base Drive Loss of a BJT



Solution

$V_{BE(sat)} = 3$ V, $I_B = 8$ A, $T = 1/f_s = 100\ \mu$s, $k = 0.5$, $kT = 50\ \mu$s, $t_d = 0.5\ \mu$s, $t_r = 1\ \mu$s, $t_n = 50 - 1.5 = 48.5\ \mu$s, $t_s = 5\ \mu$s, $t_f = 3\ \mu$s, $t_{on} = t_d + t_r = 1.5\ \mu$s, and $t_{off} = t_s + t_f = 5 + 3 = 8\ \mu$s.

During the period, $0 \le t \le (t_{on} + t_n)$:

$$i_b(t) = I_{BS}$$
$$v_{BE}(t) = V_{BE(sat)}$$

The instantaneous power due to the base current is

$$P_b(t) = i_b v_{BE} = I_{BS} V_{BS(sat)}$$
$$= 8 \times 3 = 24\ \text{W}$$

During the period, $0 \le t \le t_o = (T - t_{on} - t_n - t_s - t_f)$: $P_b(t) = 0$. The average power loss is

$$P_B = I_{BS} V_{BE(sat)} (t_{on} + t_n + t_s + t_f) f_s$$
$$= 8 \times 3 \times (1.5 + 48.5 + 5 + 3) \times 10^{-6} \times 10 \times 10^3 = 13.92\ \text{W}$$

Switching Limits

Second breakdown (SB). The SB, which is a destructive phenomenon, results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor. Thus, secondary breakdown is caused by a localized thermal runaway, resulting from high current concentrations. The current concentration may be caused by defects in the transistor structure. The SB occurs at certain combinations of voltage, current, and time. Because the time is involved, the secondary breakdown is basically an energy dependent phenomenon.

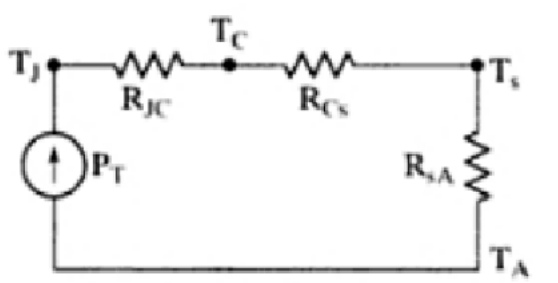
Forward-biased safe operating area (FBSOA). During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power-handling capability of a transistor. The manufacturers usually provide the FBSOA curves under specified test conditions. FBSOA indicates the $i_c - v_{CE}$ limits of the transistor; and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.

Reverse-biased safe operating area (RBSOA). During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-to-emitter junction reverse biased. The collector–emitter voltage must be held to a safe level at, or below, a specified value of collector current. The manufacturers provide the $I_C - V_{CE}$ limits during reverse-biased turn-off as RBSOA.

Power derating.

total average power loss is P_T, the case temperature is

$$T_C = T_J - P_T R_{JC}$$



Thermal equivalent circuit of a transistor.

The sink temperature is

$$T_S = T_C - P_T R_{CS}$$

The ambient temperature is

$$T_A = T_S - P_T R_{SA}$$

and

$$T_J - T_A = P_T(R_{JC} + R_{CS} + R_{SA})$$

where R_{JC} = thermal resistance from junction to case, °C/W;
R_{CS} = thermal resistance from case to sink, °C/W;
R_{SA} = thermal resistance from sink to ambient, °C/W.

The maximum power dissipation P_T is normally specified at $T_C = 25°C$. If the ambient temperature is increased to $T_A = T_{J(max)} = 150°C$, the transistor can dissipate zero power. On the other hand, if the junction temperature is $T_C = 0°C$, the device can dissipate maximum power and this is not practical. Therefore, the ambient temperature and thermal resistances must be considered when interpreting the ratings of devices. Manufacturers show the derating curves for the thermal derating and second breakdown derating.

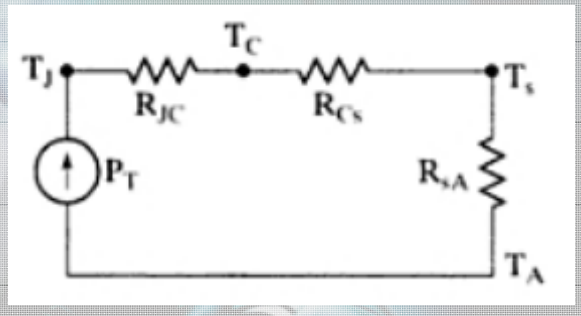
Breakdown voltages. A *breakdown voltage* is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted, or biased in either forward or reverse direction. At breakdown the voltage remains relatively constant, where the current rises rapidly. The following breakdown voltages are quoted by the manufacturers:

V_{EBO}: the maximum voltage between the emitter terminal and base terminal with collector terminal open circuited.

V_{CEV} or V_{CEX}: the maximum voltage between the collector terminal and emitter terminal at a specified negative voltage applied between base and emitter.

$V_{CEO(SUS)}$: the maximum sustaining voltage between the collector terminal and emitter terminal with the base open circuited. This rating is specified at the maximum collector current and voltage, appearing simultaneously across the device with a specified value of load inductance.

Example Finding the Case Temperature of a BJT



The maximum junction temperature of a transistor is $T_J = 150°C$ and the ambient temperature is $T_A = 25°C$. If the thermal impedances are $R_{JC} = 0.4°C/W$, $R_{CS} = 0.1°C/W$, and $R_{SA} = 0.5°C/W$, calculate (a) the maximum power dissipation, and (b) the case temperature.

Solution

a. $T_J - T_A = P_T(R_{JC} + R_{CS} + R_{SA}) = P_T R_{JA}$, $R_{JA} = 0.4 + 0.1 + 0.5 = 1.0$, and $150 - 25 = 1.0P_T$, which gives the maximum power dissipation as $P_T = 125\ W$.

b. $T_C = T_J - P_T R_{JC} = 150 - 125 \times 0.4 = 100°C$.