Impact of PWM switching on modeling of low frequency power oscillation in electrical rail vehicle

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Keywords

«Traction application», « Rail vehicle», « voltage source converter», « pulse width modulation», «Single phase system»

Abstract

For stability investigation of complex power systems, simplified system models are in need in order to reduce the model complexity and the simulation time. In this paper the effect of modelling a voltage source converter (VSC) for traction power system with and without the detailed pulse width modulated (PWM)-switch model is modeled in PSCAD and analyzed. The same disturbance is imposed for the two models and the low frequency oscillation of the DC- link voltage response is compared and analyzed. The effect of semiconductor switching on the stability limit of the system is also investigated. Furthermore, the performance of a PWM time delay compensation technique during transient is analyzed.

The result shows that in the model including the switching the DC- link voltage oscillation is damped and has a better stability limit compared to the average model. In the detailed switching model a converter loss is included while in the average model a no loss ideal case scenario is considered.

The delay in DC- link voltage control loop caused by the switching dead-time effect was improved by compensation of dead-time in the inverse-park transformation block of the control loop.The comparison of the compensated and non-compensated model proves that the compensated model is better in terms of the overshoot of amplitude of transient.

Introduction

Modern electrical locomotives are equipped with a number of power electronic equipment and advanced digital control technology. This improves the performance of the locomotive, but also introduces a lot of new dynamical phenomena of interaction with the railway power supply. For the latest years, the topic of poorly damped low frequency oscillations has been in focus. In some cases these oscillations have resulted in instability of the traction power system [1].

In order to study the interaction between the power electronic component and the rest of the railway traction power system, more realistic models have to be developed [2], [3]. In general, power system modelling includes a number of simplifications in order to reduce the model complexity and the simulation time. A typical simplification is to neglect the impact of the semiconductor switching during dynamical stability studies [4]. However in this paper the effect of the presence of semiconductor switching, which is the main source of harmonics and nonlinearity in the power

system, is considered to evaluate possible impacts on the low frequency behaviour of the system stability studies.

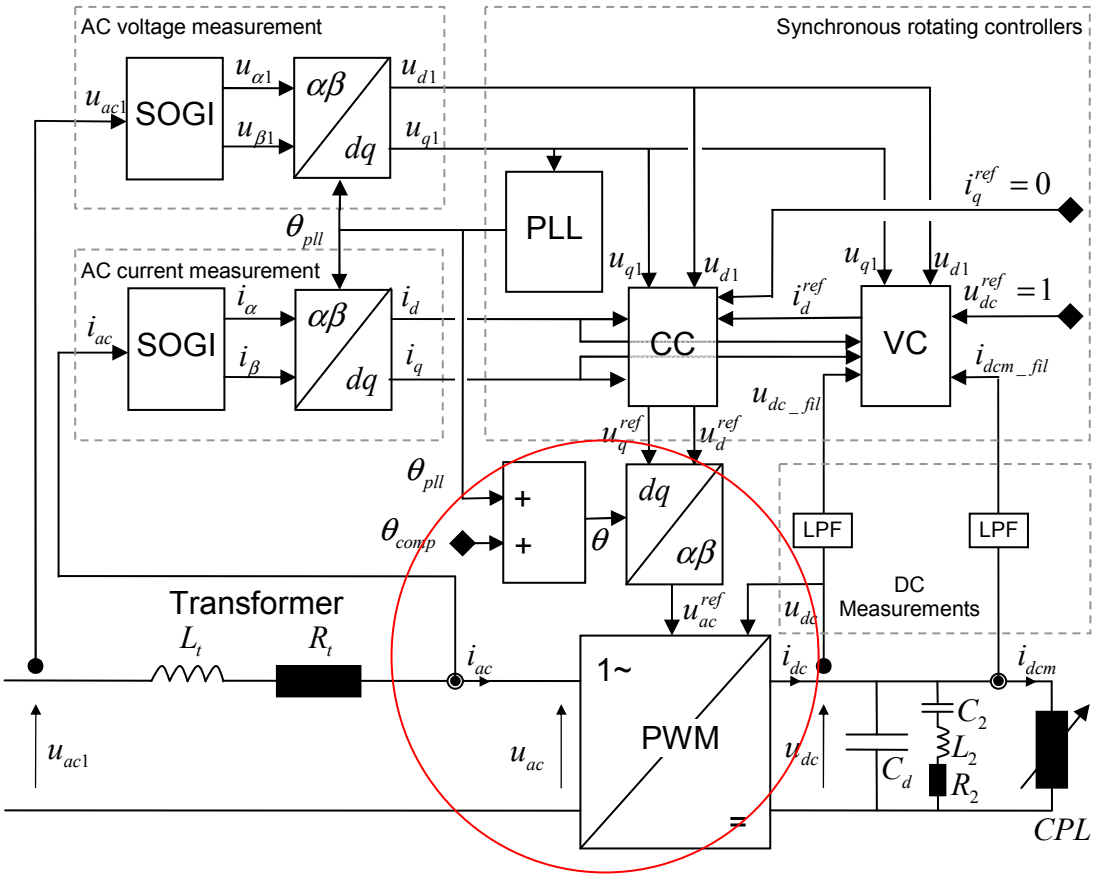

Fig 1 Single line equivalent circuit and block diagrams of the model

A VSC for traction power system with and without the detailed PWM switching model of an electrical locomotive using EMTDC/PSCAD simulation tool is made based on the simplified (average) model suggested in [4] and giving more focus on the circled area of Fig1.The detailed model takes into consideration the non-ideal pulse width modulated (PWM)-switch model with the purpose of evaluating the proposed averaged model accuracy, using the refined model for semiconductor devices, to observe the low frequency oscillation response.

The main advantage of the proposed switching model is that it takes into account the nonlinear effects of power devices and makes it possible to estimate the dissipated power in the different circuit devices and to evaluate the effect of the semiconductor devices on the general performance of the system low frequency behavior.

The averaged model is limited since the semiconductor devices nonlinearities and the simple switching and static characteristics of these devices are neglected. In this detailed semiconductor switchiching model, a non-ideal pulse width modulated switch model are considered .Moreover in this paper, the compensation technique proposed in [5] is used to compensate for the delay caused by the dead-time of the switching devices.

System model description

The system under study is a single-phase PWM inverter connecting a simple AC-system and a simple DC-system as shown in Fig 2. The AC- system includes: an ideal voltage source for 16 2/3 Hz having

amplitude of $\sqrt{2} \cdot 16.5$ kV, a 60 km overhead contact line having impedance of (0.19+j0.21) Ω/km and the vehicle main 15 kV/1.558 kV step down transformer.

The DC-system reflects the vehicle DC-link with the DC-link capacitance C_d of 40 mF, the second harmonic resonance tank C_2, L_2 and R_2 tuned on 33.4 Hz in order to reduce the second harmonic ripple given by the single-phase system power pulsations, a constant power load (*CPL*) drawing a current i_{dcm} (see equation (1)) as a simplified equivalent for the motor side.

$$i_{dcm}(t) = P_m^{ref}(t) / u_{dc}(t) \tag{1}$$

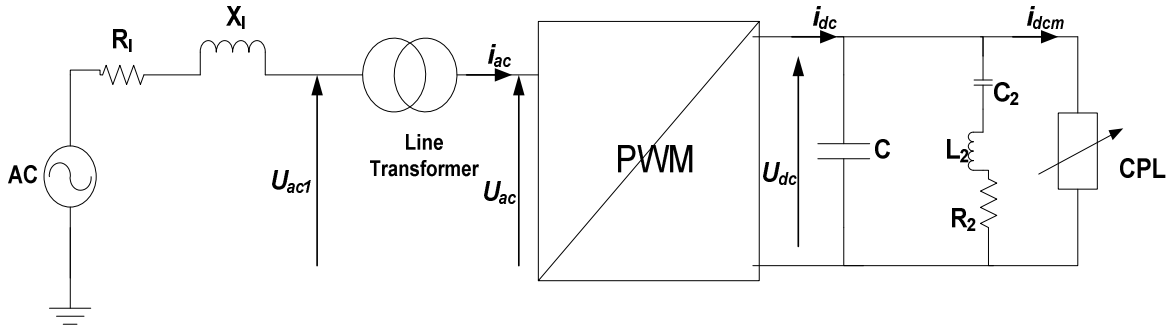

Fig 2 : Schematic representation of the electrical system under investigation.

The control system for the line inverter consists of the synchronization controller which is a phase locked loop (*PLL*) that constantly tracks the phase of the line voltage u_{ac1} for orientation of the direct (*d*) and quadrature (*q*) axis reference frame in which the other controllers rotate. A second-order generalized integrator (*SOGI*) [6] is used for generation of an artificial orthogonal voltage as input to the *PLL*.

The DC-link voltage proportional-integral controller *VC* compares the measured DC-link voltage u_{dc_fil} to its constant reference and together with the fed forward measured motor current i_{dcm_fil} calculates the active current reference i_{dref} for the current controller based on the ratio between the measured DC and AC voltages, u_{dc_fil} and u_{d1} respectively (see Fig 1).

The AC-current proportional-integral controllers (*CC*) compare the measured *d*- and *q*-axis (i_d and i_q) to the respective active and reactive current references i_d^{ref} and i_q^{ref}. The two axes are decoupled over the transformer impedance X_t in order to allow independent control of active and reactive power. The reactive power is controlled to be zero at the vehicle transformer line side, i.e. i_{ac} in phase with u_{ac1}.

A detailed switching model of single-phase PWM inverter with a triangular carrier frequency of 250Hz and a reference voltage of u_{ac}^{ref} with unipolar voltage switching technique is included for the switching model. In railway application system it is common to use the unipolar voltage switching. This type of switching has the advantage of doubling the effective switching frequency as far as the output harmonics are concerned, compared to the bipolar switching scheme [7], [8] .

In the average model, Fig 3, the PWM is simplified into a controlled current source that calculates the current based on the AC-side power divided by the DC-link voltage, at the converter DC-side of the model, v_{dc} at shown in equation (2).

$$i_{av}(t) = [i_{ac}(t) * u_{ac}(t)] / u_{dc}(t) \tag{2}$$

In the converter AC-side the PWM is simplified by a controlled voltage source which is controlled by the reference AC-voltage from the inverse park transformation block output u_{ac}^{ref} .

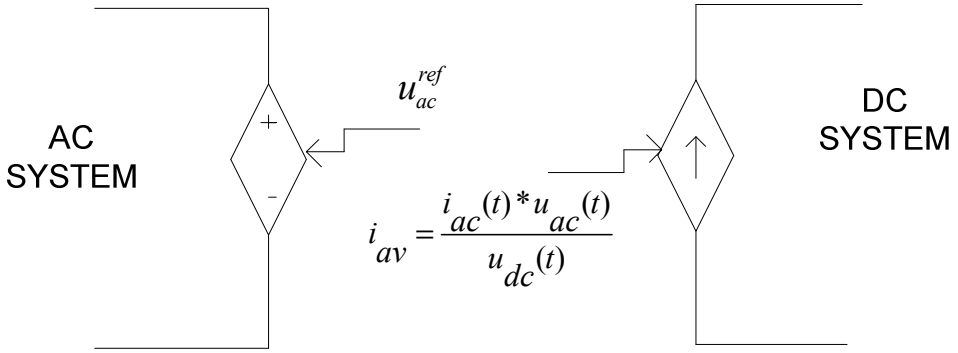

Fig 3 : Schematic representation of the PWM in the average model.

In addition, a *SOGI* is used for measurement of the line current i_{ac} as well. First-order low-pass filters are used for measurement of the u_{dc} and i_{dcm} .

Dead-time delay compensation technique

The up to date technology in motor control provides an adjustable voltage and frequency to the terminals of the motor through a pulse width modulated (PWM) voltage source inverter drive. In this type of drives, a dead-time exists due to non-ideal characteristic of power switching devices. Although the dead-time is short, it causes deviations from the desired fundamental output voltage. Despite the fact that each deviation does not significantly affect the fundamental voltage, the accumulated deviations result in reduced fundamental output voltage, distorted machine currents, and torque pulsations. The dead-time problem has already been investigated and several techniques of compensation has been proposed [9], [10].

For triangular carrier modulators, an average time delay from the reference voltage u_{ac}^{ref} to the actuated PWM terminal voltage u_{ac1} of half the switching frequency is assumed [11]. This average delay can be compensated by manipulating the synchronous rotating reference frame angle θ_{pll} as proposed in [5].

The analysis in [5] shows that the correction can be implemented as a modified $\alpha\beta$ transformation. It is also possible to implement a stand-alone correction, $v_{corr}(t)$,as in equation (3) and (4).where the inverter command vector is denoted as *v (t)*.

$$v_{corr}(t) = e^{j\omega 1(t)\tau} v(t) \tag{3}$$

On real-value vector form:

$$v_{corr}(t) = \begin{pmatrix} \cos\omega_1(t)\tau & \sin\omega_1(t)\tau \\ -\sin\omega_1(t)\tau & \cos\omega_1(t)\tau \end{pmatrix} v(t) \tag{4}$$

The compensation angle, θ_{comp}, in equation (5) for $\tau = \frac{1}{2}T_{sw}$ and $\omega_1(t) = 2\pi f_1$ is given by the switching frequency f_{sw} and the fundamental frequency, f_1, as shown in equation (6). This angle is compensated for the pulse width modulated (PWM)-switch model in *dq* to *αβ* transformation block as shown in the circled area of Fig 1.

$$\theta_{comp} = \omega_1(t)\tau\,[rad] \tag{5}$$

$$\theta_{comp} = \frac{\pi f_1}{f_{sw}}[rad] \tag{6}$$

Simulation results

Comparison of switching and average models

The result shown in Fig 4 compares the average model and the switching model of the DC-link voltage when a 3.67MW step in motor power is added at 60km line. In both curves it is observed the typical second harmonic ripple twice the line frequency as expected in this case. In addition, in the switching model a ripple due to the semiconductor switching which is twice the switching frequency due to use of unipolar voltage switching is observed.

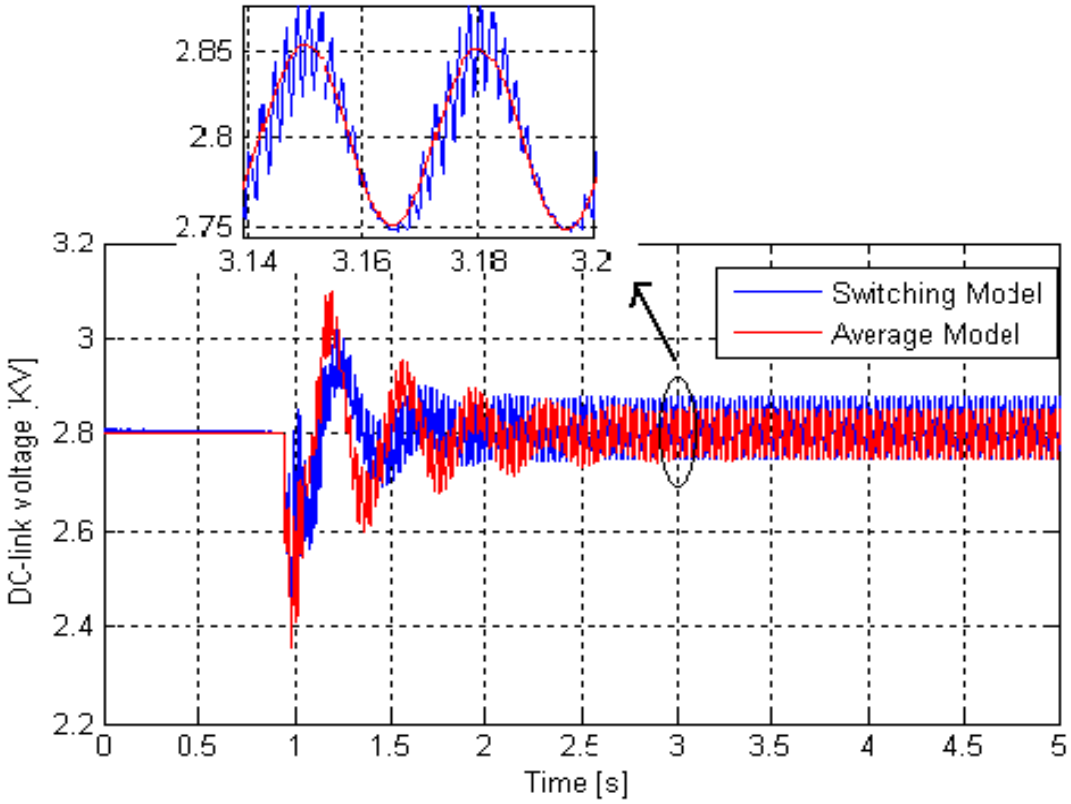

Fig 4 : Response in DC-link voltage when a 3.67MW step in motor power is added at 60km line for the two models.

In order to see the low frequency behavior of this response for the two models Fig 4 is averaged in a period of $T = 1/f_1[\text{sec}]$ and is shown in Fig 5.

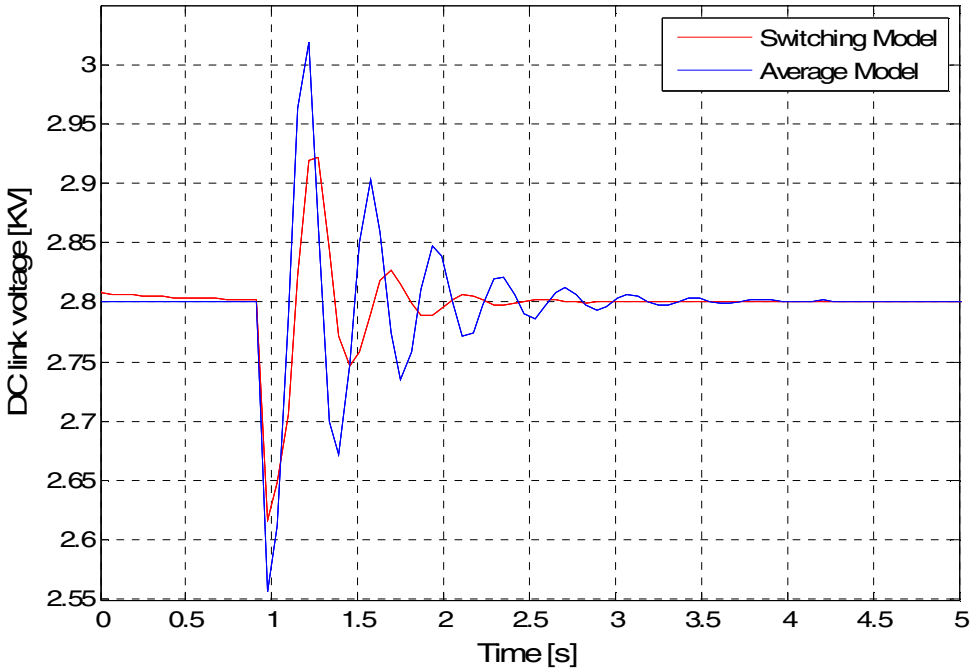

Fig 5 : Low frequency oscillation of DC-link voltage compared for the two models.

Table 1: Comparison of switching and average models

	Average model	Switching model
Settling time	2.5seconds	1.5seconds
Frequency of oscillation	2.67Hz	2Hz

The frequency of oscillation and the settling time for the switching and average model is calculated and given in Table 1. As we can see in the table the switching model has a better damping, less settling time and lower amplitude overshoot (Fig 5).

In the switching model the losses in the converter (the averaged dissipated power $P_D(t)$ in the semiconductor devices) can be obtained by subtracting the power output, $P_{output}(t)$, from the converter to the power input, $P_{input}(t)$, to the converter as shown in equation (7).

$$P_D(t) = P_{input}(t) - P_{output}(t) \tag{7}$$

This loss when the load consumes 3.67MW power is calculated in PSCAD and shown in Fig 6. The converter has a loss of 0.218MW which is 6% of the total power. A first-order low-pass filter is used for measurement of the loss.

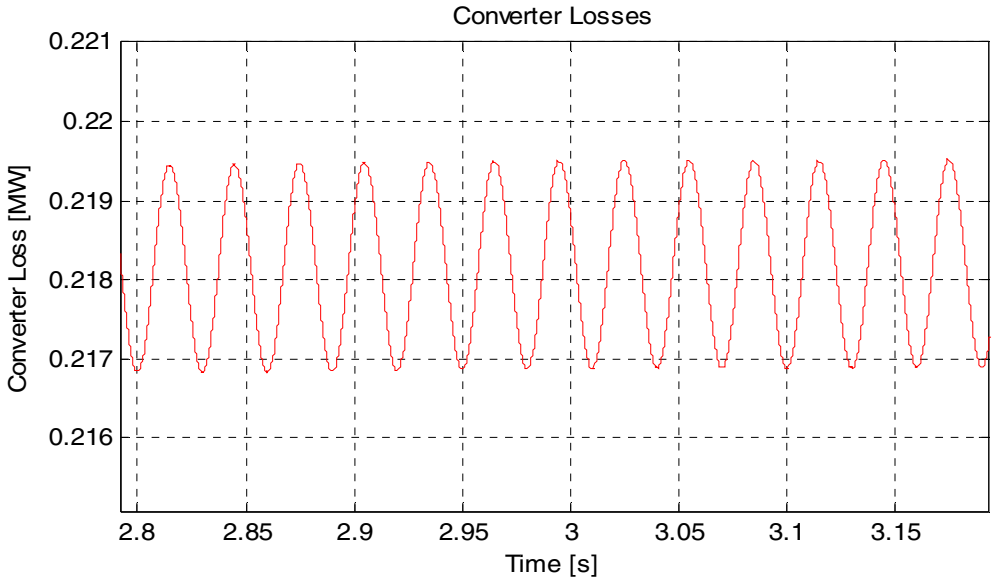

Fig 6: Calculated converter loss by equation (7) in PSCAD.

Stability limit investigation for average and switching models

For the purpose of investigating the stability limit of the models a time simulation method is carried out in EMTDC/PSCAD. The line length is increased by increasing the line parameters in the model. Fig 7 shows the DC- link voltage measurement for different line lengths at no load scenario. The line is increased in both the switching model and average model and the plots are shown in the right and left side of Fig 7 respectively.

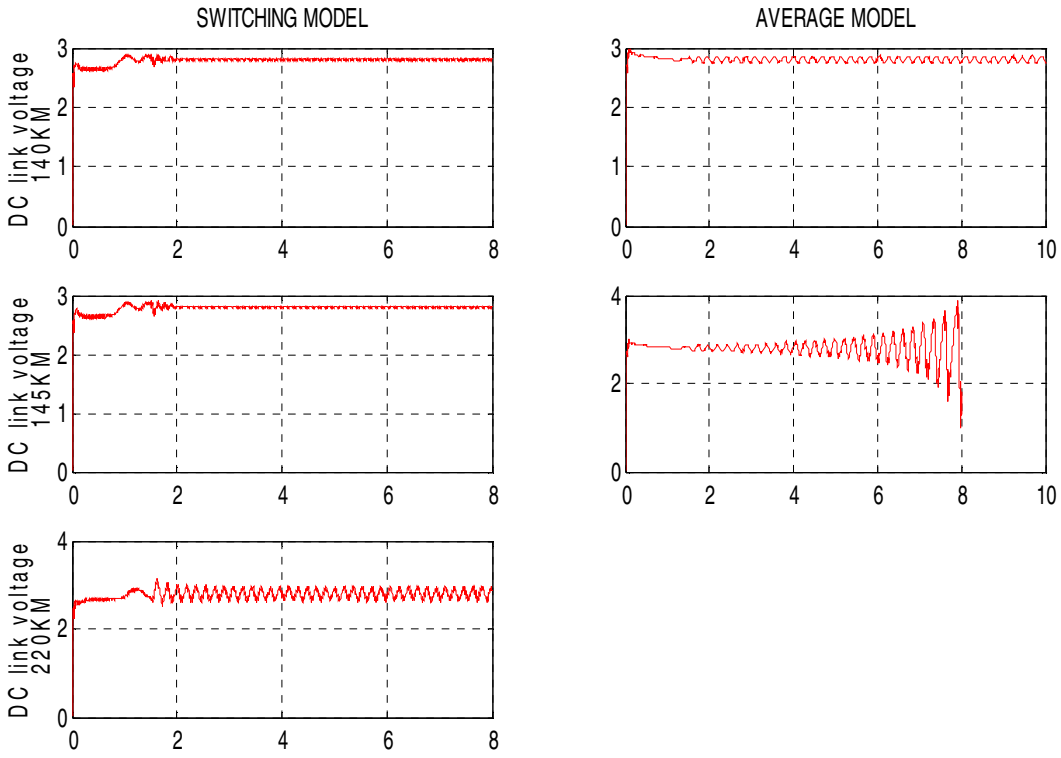

Fig 7 : Stability limit investigation on the average and switching model

The result in the figure shows at 145km the average model DC-link voltage is oscillating and the amplitude of oscillation is growing. This is DC-link voltage instability. However, at the same line length the switching model DC-link voltage is well damped.

In the low frequency oscillation comparison shown previously in Fig 5 the switching model is more damped and has lower overshoot compared to the average model. This result agrees with the stability limit investigated in Fig 7, which gives the switching model a longer stability limit.

The switching model has a detail converter model which adds 6% converter loss as described in the previous section. The phenomenon which adds a damping effect is not well understood, however this analysis proves that the switching of the semiconductor adds a damping effect on the low frequency behavior of the system.

Comparison of the dead-time compensated and non-compensated models

Fig 8 shows the comparison of DC-link voltage response for a 3.67MW step in motor power between the dead-time compensated model and non-compensated model.

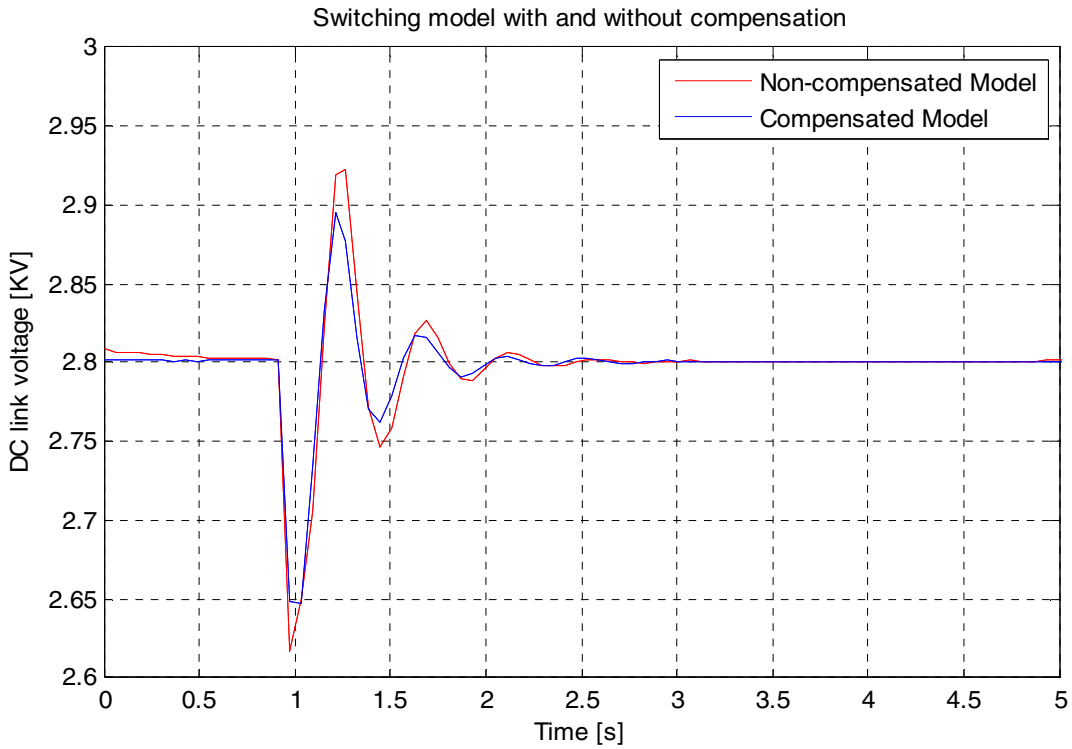

Fig 8: DC-link voltage response with and without the dead-time compensation.

The simulation is carried out to improve the delay in DC- link voltage control loop caused by the switching dead-time by using the proposed compensation method in the inverse-park transformation block of the control loop.

Comparison of the dead-time compensated and non-compensated models is shown in Fig 8. The delay is compensated during transients as can be seen from the figure and can be neglected in the average model since semiconductor switching is not included in the simplified model. Moreover, the delay in DC- link voltage control loop caused by the switching dead-time effect was improved in terms of transient overshoot by compensation of dead-time in the inverse-park transformation block of the control loop.

Conclusion

In this paper VSC for traction power system with and without including the detailed PWM switching is modeled. The effect of semiconductor switching on the low frequency behavior of the DC-link voltage when a 3.67MW step power is added at 60km line is investigated. Furthermore, the performance of a PWM time delay compensation technique is analyzed.

From the presented results, the average model gives less realistic representation of the converter dynamics concerning transient oscillations. Therefore the detailed model with the PWM switching gives an improved representation of the system from the low frequency behavior point of view. Moreover, the delay in DC- link voltage control loop caused by the switching dead-time effect was improved by compensation of dead-time in the inverse-park transformation block of the control loop.

In order to study the low frequency behavior for stability limit investigation of a traction systems, a detailed semiconductor switching (PWM) - model, which takes into account the semiconductor nonlinearity needs to be modeled and well understood. The same investigation could also be done with the average model by including an equivalent representation of the effect of the switching action that can give the same low frequency response as in the detailed switching model.

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