In The Name Of God

Power Electronics

Inverters

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Pulse-Width-Modulated Inverters

The learning objectives of this chapter are as follows:

- To learn the switching technique for dc–ac converters known as inverters and the types of inverters
- To study the operation of inverters
- To understand the performance parameters of inverters
- To learn the different types of modulation techniques to obtain a near sinusoidal output waveform and the techniques to eliminate certain harmonics from the output
- To learn the techniques for analyzing and designing inverters and for simulating inverters by using SPICE
- To study the effects of load impedance on the load current

INTRODUCTION

Dc-to-ac converters are known as *inverters*. The function of an inverter is to change a dc input voltage to a symmetric ac output voltage of desired magnitude and frequency [1]. The output voltage could be fixed or variable at a fixed or variable frequency. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. On the other hand, if the dc input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter. The *inverter gain* may be defined as the ratio of the ac output voltage to dc input voltage.

The output voltage waveforms of ideal inverters should be sinusoidal. However, the waveforms of practical inverters are nonsinusoidal and contain certain harmonics. For low- and medium-power applications, square-wave or quasi-square-wave voltages may be acceptable; and for high-power applications, low distorted sinusoidal waveforms are required. With the availability of high-speed power semiconductor devices, the harmonic contents of output voltage can be minimized or reduced significantly by switching techniques.

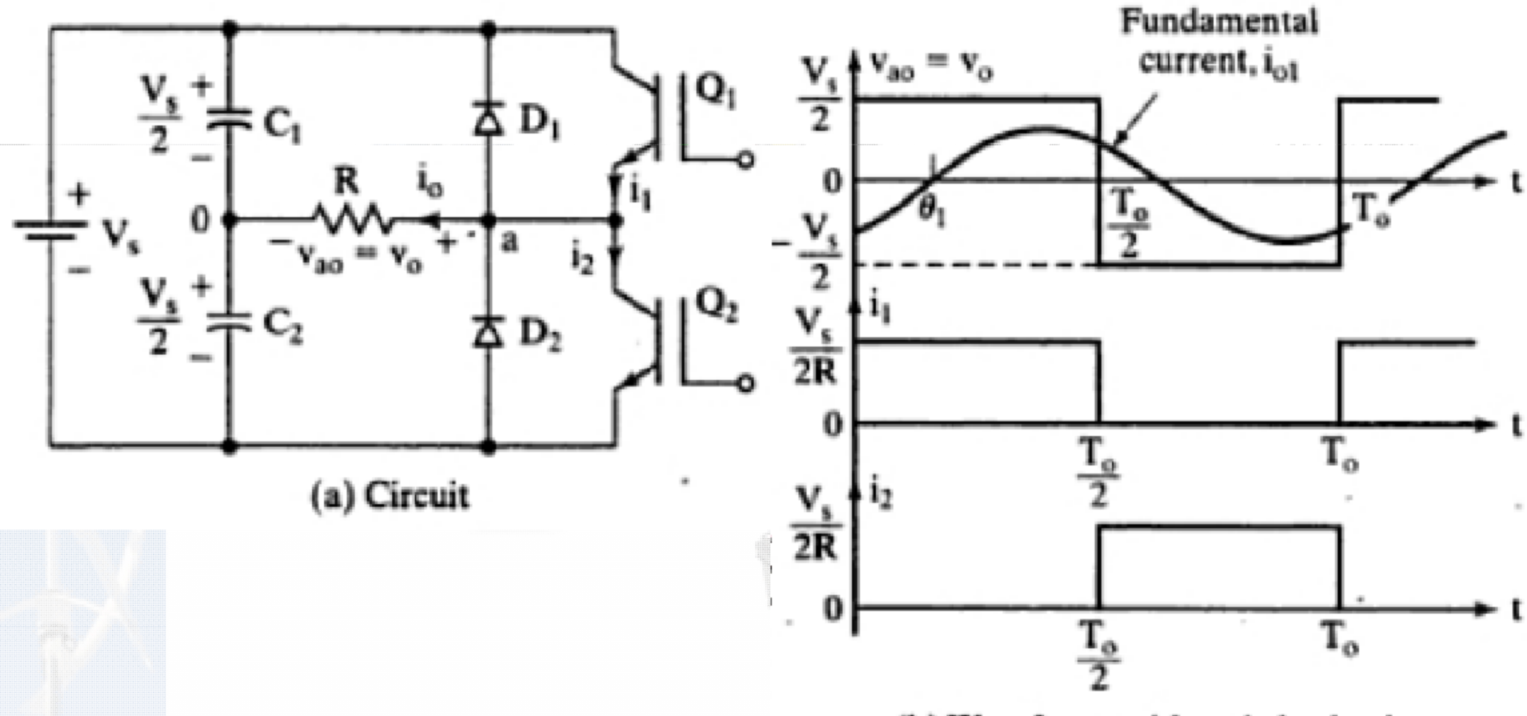
Inverters are widely used in industrial applications (e.g., variable-speed ac motor drives, induction heating, standby power supplies, and uninterruptible power supplies). The input may be a battery, fuel cell, solar cell, or other dc source. The typical single-phase outputs are (1) 120 V at 60 Hz, (2) 220 V at 50 Hz, and (3) 115 V at 400 Hz. For high-power three-phase systems, typical outputs are (1) 220 to 380 V at 50 Hz, (2) 120 to 208 V at 60 Hz, and (3) 115 to 200 V at 400 Hz.

UG R600 Wind Turbine (600W)

Inverters can be broadly classified into two types: (1) single-phase inverters, and (2) three-phase inverters. Each type can use controlled turn-on and turn-off devices (e.g., bipolar junction transistors [BJTs], metal oxide semiconductor field-effect transistors [MOSFETs], insulated-gate bipolar transistors [IGBTs], metal oxide semiconductor-controlled thyristors [MCTs], static induction transistors, [SITs], and gate-turn-off thyristors [GTOs]). These inverters generally use PWM control signals for producing an ac output voltage. An inverter is called a *voltage-fed inverter* (VFI) if the input voltage remains constant, a *current-fed inverter* (CFI) if the input current is maintained constant, and a *variable dc linked inverter* if the input voltage is controllable. If the output voltage or current of the inverter is forced to pass through zero by creating an *LC* resonant circuit, this type of inverter is called *resonant-pulse inverter* and it has wide applications in power electronics. Chapter 8 is devoted to resonant-pulse inverters only.

PRINCIPLE OF OPERATION

The principle of single-phase inverters [1] can be explained with Figure 6.1a. The inverter circuit consists of two choppers. When only transistor Q_1 is turned on for a time $T_0/2$, the instantaneous voltage across the load v_0 is $V_s/2$. If transistor Q_2 only is turned on for a time $T_0/2$, $-V_s/2$ appears across the load. The logic circuit should be designed such that Q_1 and Q_2 are not turned on at the same time. Figure 6.1b shows the waveforms for the output voltage and transistor currents with a resistive load. This inverter requires a three-wire dc source, and when a transistor is off, its reverse voltage is V_s instead of $V_s/2$. This inverter is known as a *half-bridge inverter*.



(a) Circuit

(b) Waveforms with resistive load

The root-mean-square (rms) output voltage can be found from

$$V_o = \left(\frac{2}{T_0}\int_0^{T_0/2}\frac{V_s^2}{4}\,dt\right)^{1/2} = \frac{V_s}{2} \tag{6.1}$$

The instantaneous output voltage can be expressed in Fourier series as

$$v_o = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left(a_n\cos(n\omega t) + b_n\sin(n\omega t)\right)$$

Due to the quarter-wave symmetry along the x-axis, both a_0 and a_n are zero. We get b_n as

$$b_n = \frac{1}{\pi}\left[\int_{-\frac{\pi}{2}}^{0}\frac{-V_s}{2}\,d(\omega t) + \int_0^{\frac{\pi}{2}}\frac{V_s}{2}\,d(\omega t)\right] = \frac{4V_s}{n\pi}$$

which gives the instantaneous output voltage v_o as

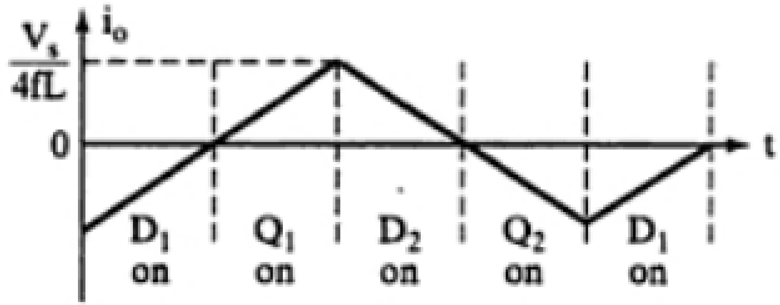
$$v_0 = \sum_{n=1,3,5,\ldots}^{\infty}\frac{2V_s}{n\pi}\sin n\omega t$$

$$= 0 \qquad \text{for } n = 2, 4, \ldots \tag{6.2}$$

where $\omega = 2\pi f_0$ is the frequency of output voltage in rads per second. Due to the quarter-wave symmetry of the output voltage along the x-axis, the even harmonics voltages are absent. For $n = 1$, Eq. (6.2) gives the rms value of fundamental component as

$$V_{o1} = \frac{2V_s}{\sqrt{2}\pi} = 0.45V_s \tag{6.3}$$

For an inductive load, the load current cannot change immediately with the output voltage. If Q_1 is turned off at $t = T_0/2$, the load current would continue to flow through D_2, load, and lower half of the dc source until the current falls to zero. Similary, when Q_2 is turned off at $t = T_0$, the load current flows through D_1, load, and upper half of the dc source. When diode D_1 or D_2 conducts, energy is fed back to the dc source and these diodes are known as *feedback diodes*. Figure 6.1c shows the load current and conduction intervals of devices for a purely inductive load. It can be noticed that for a purely inductive load, a transistor conducts only for $T_0/2$ (or 90°). Depending on the load impedance angle, the conduction period of a transistor would vary from 90° to 180°.



(c) Load current with highly inductive load

Any switching devices can replace the transistors. If t_{off} is the turn-off time of a device, there must be a minimum delay time of $t_d(= t_{off})$ between the outgoing device and triggering of the next incoming device. Otherwise, short-circuit condition would result through the two devices. Therefore, the maximum conduction time of a device would be $t_{on} = T_o/2 - t_d$. All practical devices require a certain turn-on and turn-off time. For successful operation of inverters, the logic circuit should take these into account.

For an RL load, the instantaneous load current i_0 can be found by dividing the instantaneous output voltage by the load impedance $Z = R + jn\omega L$. Thus, we get

$$i_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \theta_n) \tag{6.4}$$

where $\theta_n = \tan^{-1}(n\omega L/R)$. If I_{01} is the rms fundamental load current, the fundamental output power (for $n = 1$) is

$$P_{01} = V_{o1} I_{01} \cos\theta_1 = I_{01}^2 R \tag{6.5}$$

$$= \left[\frac{2V_s}{\sqrt{2}\pi\sqrt{R^2 + (\omega L)^2}}\right]^2 R \tag{6.5a}$$

Note: In most applications (e.g., electric motor drives) the output power due to the fundamental current is generally the useful power, and the power due to harmonic currents is dissipated as heat and increases the load temperature.

Dc supply current. Assuming a lossless inverter, the average power absorbed by the load must be equal to the average power supplied by the dc source. Thus, we can write

$$\int_0^T v_s(t) i_s(t) dt = \int_0^T v_o(t) i_o(t) dt$$

where T is the period of the ac output voltage. For an inductive load and a relatively high switching frequency, the load current i_o is nearly sinusoidal; therefore, only the fundamental component of the ac output voltage provides power to the load. Because the dc supply voltage remains constant $v_s(t) = V_s$, we can write

$$\int_0^T i_s(t) dt = \frac{1}{V_s} \int_0^T \sqrt{2} V_{o1} \sin(\omega t) \sqrt{2} I_o \sin(\omega t - \theta_1) dt = I_s$$

where V_{o1} is the fundamental rms output voltage;
I_o is the rms load current;
θ_1 is the load angle at the fundamental frequency.

Thus, the dc supply current I_s can be simplified to

$$I_s = \frac{V_{o1}}{V_s} I_o \cos(\theta_1) \tag{6.6}$$

Key Points of Section 6.2

- An ac output voltage can be obtained by alternatively connecting the positive and negative terminals of the dc source across the load by turning on and off the switching devices accordingly. The rms fundamental component V_{o1} of the output voltage is $0.45\ V_s$.
- Feedback diodes are required to transfer the energy stored in the load inductance back to the dc source.

PERFORMANCE PARAMETERS

The output of practical inverters contain harmonics and the quality of an inverter is normally evaluated in terms of the following performance parameters.

Harmonic factor of nth harmonic (HF_n). The harmonic factor (of the nth harmonic), which is a measure of individual harmonic contribution, is defined as

$$HF_n = \frac{V_{on}}{V_{o1}} \qquad \text{for } n > 1 \tag{6.7}$$

where V_1 is the rms value of the fundamental component and V_{on} is the rms value of the nth harmonic component.

Total harmonic distortion (THD). The total harmonic distortion, which is a measure of closeness in shape between a waveform and its fundamental component, is defined as

$$\text{THD} = \frac{1}{V_{o1}}\left(\sum_{n=2,3,\ldots}^{\infty} V_{on}^2\right)^{1/2} \tag{6.8}$$

Distortion factor (DF). THD gives the total harmonic content, but it does not indicate the level of each harmonic component. If a filter is used at the output of inverters, the higher order harmonics would be attenuated more effectively. Therefore, a knowledge of both the frequency and magnitude of each harmonic is important. The DF indicates the amount of HD that remains in a particular waveform after the harmonics of that waveform have been subjected to a second-order attenuation (i.e., divided by n^2). Thus, DF is a measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second-order load filter and is defined as

$$\text{DF} = \frac{1}{V_{o1}}\left[\sum_{n=2,3,\ldots}^{\infty}\left(\frac{V_{on}}{n^2}\right)^2\right]^{1/2} \tag{6.9}$$

The DF of an individual (or nth) harmonic component is defined as

$$DF_n = \frac{V_{on}}{V_{o1} n^2} \quad \text{for } n > 1 \tag{6.10}$$

Lowest order harmonic (LOH). The LOH is that harmonic component whose frequency is closest to the fundamental one, and its amplitude is greater than or equal to 3% of the fundamental component.

Example 6.1 Finding the Parameters of the Single-Phase Half-Bridge Inverter

The single-phase half-bridge inverter in Figure 6.1a has a resistive load of $R = 2.4\ \Omega$ and the dc input voltage is $V_s = 48$ V. Determine (a) the rms output voltage at the fundamental frequency V_{o1}, (b) the output power P_o, (c) the average and peak currents of each transistor, (d) the peak reverse blocking voltage V_{BR} of each transistor, (e) the THD, (f) the DF, and (g) the HF and DF of the LOH.

Solution

$V_s = 48$ V and $R = 2.4\ \Omega$.

a. From Eq. (6.3), $V_{o1} = 0.45 \times 48 = 21.6$ V.

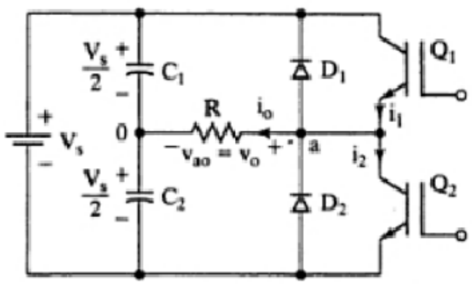
b. From Eq. (6.1), $V_o = V_s/2 = 48/2 = 24$ V. The output power, $P_o = V_o^2/R = 24^2/2.4 = 240$ W.

c. The peak transistor current $I_p = 24/2.4 = 10$ A. Because each transistor conducts for a 50% duty cycle, the average current of each transistor is $I_Q = 0.5 \times 10 = 5$ A.

d. The peak reverse blocking voltage $V_{BR} = 2 \times 24 = 48$ V.

e. From Eq. (6.3), $V_{o1} = 0.45V_s$ and the rms harmonic voltage V_h

$$V_h = \left(\sum_{n=3,5,7,\ldots}^{\infty} V_{on}^2\right)^{1/2} = (V_o^2 - V_{o1}^2)^{1/2} = 0.2176V_s$$



(a) Circuit

From Eq. (6.8), THD $= (0.2176V_s)/(0.45V_s) = 48.34\%$.

f. From Eq. (6.2), we can find V_{on} and then find,

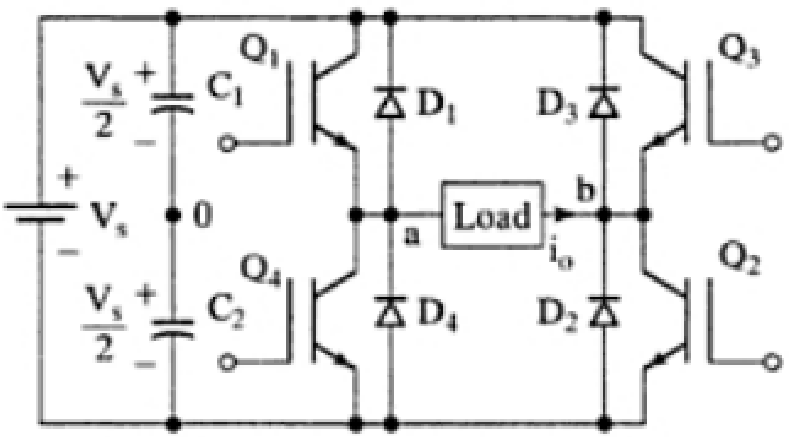
$$\left[\sum_{n=3,5,\ldots}^{\infty}\left(\frac{V_{on}}{n^2}\right)^2\right]^{1/2} = \left[\left(\frac{V_{o3}}{3^2}\right)^2 + \left(\frac{V_{o5}}{5^2}\right)^2 + \left(\frac{V_{o7}}{7^2}\right)^2 + \cdots\right]^{1/2} = 0.024V_s$$

From Eq. (6.9), DF $= 0.024V_s/(0.45V_s) = 5.382\%$.

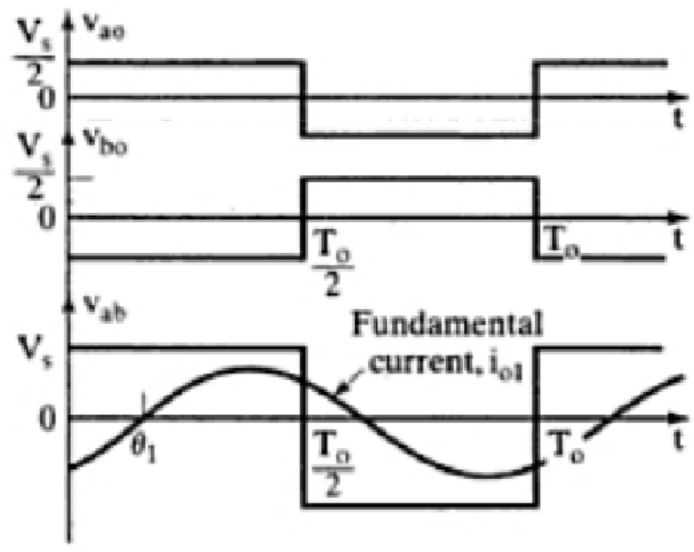
g. The LOH is the third, $V_{o3} = V_{o1}/3$. From Eq. (6.7), $HF_3 = V_{o3}/V_{o1} = 1/3 = 33.33\%$, and from Eq. (6.10), $DF_3 = (V_{o3}/3^2)/V_{o1} = 1/27 = 3.704\%$. Because $V_{o3}/V_{o1} = 33.33\%$, which is greater than 3%, LOH $= V_{o3}$.

SINGLE-PHASE BRIDGE INVERTERS

A single-phase bridge voltage source inverter (VSI) is shown in Figure 6.2a. It consists of four choppers. When transistors Q_1 and Q_2 are turned on simultaneously, the input voltage V_s appears across the load. If transistors Q_3 and Q_4 are turned on at the same time, the voltage across the load is reversed and is $-V_s$. The waveform for the output voltage is shown in Figure 6.2b.



(a) Circuit



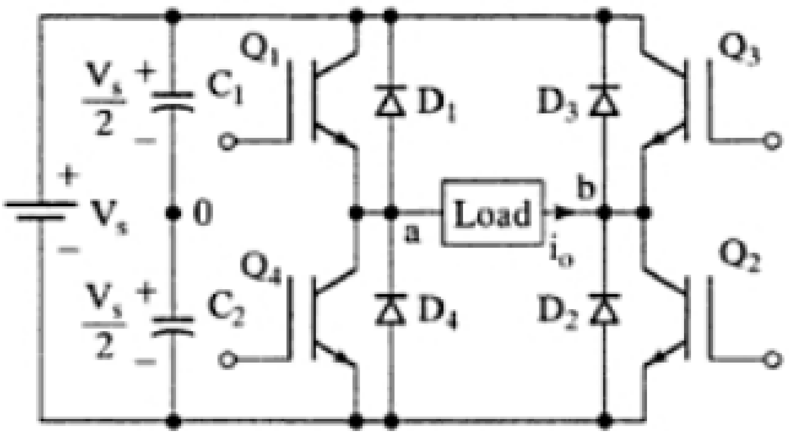
(b) Waveforms

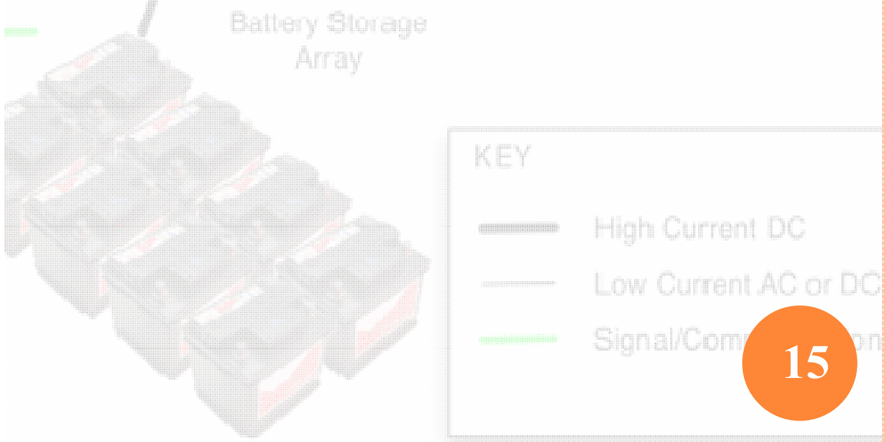
Table 6.1 shows the five switch states. Transistors Q_1, Q_4 in Figure 6.2a act as the switching devices S_1, S_4, respectively. If two switches: one upper and one lower conduct at the same time such that the output voltage is $\pm V_s$, the switch state is 1, whereas if these switches are off at the same time, the switch state is 0.

TABLE 6.1 Switch States for a Single-Phase Full-Bridge Voltage-Source Inverter (VSI)

State	State No.	Switch State*	v_{ao}	v_{bo}	v_o	Components Conducting
S_1 and S_2 are on and S_4 and S_3 are off	1	10	$V_S/2$	$-V_S/2$	V_S	S_1 and S_2 if $i_o > 0$ D_1 and D_2 if $i_o < 0$
S_4 and S_3 are on and S_1 and S_2 are off	2	01	$-V_S/2$	$V_S/2$	$-V_S$	D_4 and D_3 if $i_o > 0$ S_4 and S_3 if $i_o < 0$
S_1 and S_3 are on and S_4 and S_2 are off	3	11	$V_S/2$	$V_S/2$	0	S_1 and D_3 if $i_o > 0$ D_1 and S_3 if $i_o < 0$
S_4 and S_2 are on and S_1 and S_3 are off	4	00	$-V_S/2$	$-V_S/2$	0	D_4 and S_2 if $i_o > 0$ S_4 and D_2 if $i_o < 0$
S_1, S_2, S_3, and S_4 are all off	5	off	$-V_S/2$ $V_S/2$	$V_S/2$ $-V_S/2$	$-V_S$ V_S	D_4 and D_3 if $i_o > 0$ D_1 and D_2 if $i_o < 0$

* 1 if an upper switch is on and 0 if a lower switch is on.





The rms output voltage can be found from

$$V_o = \left(\frac{2}{T_0}\int_0^{T_0/2} V_s^2\, dt\right)^{1/2} = V_s \tag{6.11}$$

Equation (6.2) can be extended to express the instantaneous output voltage in a Fourier series as

$$v_o = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin n\omega t \tag{6.12}$$

and for $n = 1$, Eq. (6.12) gives the rms value of fundamental component as

$$V_1 = \frac{4V_s}{\sqrt{2}\pi} = 0.90V_s \tag{6.13}$$

Using Eq. (6.4), the instantaneous load current i_0 for an RL load becomes

$$i_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \theta_n) \tag{6.14}$$

where $\theta_n = \tan^{-1}(n\omega L/R)$.

When diodes D_1 and D_2 conduct, the energy is fed back to the dc source; thus, they are known as *feedback diodes*. Figure 6.2c shows the waveform of load current for an inductive load.

Dc supply current. Neglecting any losses, the instantaneous power balance gives,

$$v_s(t)i_s(t) = v_o(t)i_o(t)$$

For inductive load and relatively high-switching frequencies, the load current i_o and the output voltage may be assumed sinusoidal. Because the dc supply voltage remains constant $v_s(t) = V_s$, we get

$$i_s(t) = \frac{1}{V_s}\sqrt{2}V_{o1}\sin(\omega t)\sqrt{2}I_o\sin(\omega t - \theta_1)$$

which can be simplified to find the dc supply current as

$$i_s(t) = \frac{V_{o1}}{V_s}I_o\cos(\theta_1) - \frac{V_{o1}}{V_s}I_o\cos(2\omega t - \theta_1) \qquad (6.15)$$

where V_{o1} is the fundamental rms output voltage;
I_o is the rms load current;
θ_1 is the load impedance angle at the fundamental frequency.

Equation (6.15) indicates the presence of a second-order harmonic of the same order of magnitude as the dc supply current. This harmonic is injected back into the dc voltage source. Thus, the design should consider this to guarantee a nearly constant dc link voltage. A large capacitor is normally connected across the dc voltage source and such a capacitor is costly and demands space; both features are undesirable, especially in medium to high power supplies.

Example 6.2 Finding the Parameters of the Single-Phase Full-Bridge Inverter

Repeat Example 6.1 for a single-phase bridge inverter in Figure 6.2a.

Solution

$V_s = 48$ V and $R = 2.4\ \Omega$.

a. From Eq. (6.13), $V_1 = 0.90 \times 48 = 43.2$ V.

b. From Eq. (6.11), $V_o = V_s = 48$ V. The output power is $P_o = V_s^2/R = 48^2/2.4 = 960$ W.

c. The peak transistor current is $I_p = 48/2.4 = 20$ A. Because each transistor conducts for a 50% duty cycle, the average current of each transistor is $I_Q = 0.5 \times 20 = 10$ A.

d. The peak reverse blocking voltage is $V_{BR} = 48$ V.

e. From Eq. (6.13), $V_1 = 0.9V_s$. The rms harmonic voltage V_h is

$$V_h = \left(\sum_{n=3,5,7,\ldots}^{\infty} V_{on}^2 \right)^{1/2} = (V_0^2 - V_{01}^2)^{1/2} = 0.4352V_s$$

From Eq. (6.8), THD $= 0.4359V_s/(0.9V_s) = 48.34\%$.

f. $$\left[\sum_{n=3,5,7,\ldots}^{\infty} \left(\frac{V_{on}}{n^2} \right)^2 \right]^{1/2} = 0.048V_s$$

From Eq. (6.9), DF $= 0.048V_s/(0.9V_s) = 5.382\%$.

g. The LOH is the third, $V_3 = V_1/3$. From Eq. (6.7), $HF_3 = V_{o3}/V_{o1} = 1/3 = 33.33\%$ and from Eq. (6.10), $DF_3 = (V_{o3}/3^2)/V_{o1} = 1/27 = 3.704\%$.

Note: The peak reverse blocking voltage of each transistor and the quality of output voltage for half-bridge and full-bridge inverters are the same. However, for full-bridge inverters, the output power is four times higher and the fundamental component is twice that of half-bridge inverters.

Example 6.3 Finding the Output Voltage and Current of a Single-Phase Full-Bridge Inverter with an *RLC* Load

The bridge inverter in Figure 6.2a has an *RLC* load with $R = 10\ \Omega$, $L = 31.5$ mH, and $C = 112\ \mu$F. The inverter frequency is $f_0 = 60$ Hz and dc input voltage is $V_s = 220$ V. (a) Express the instantaneous load current in Fourier series. Calculate (b) the rms load current at the fundamental frequency I_{o1}; (c) the THD of the load current; (d) the power absorbed by the load P_0 and the fundamental power P_{01}; (e) the average current of dc supply I_s; and (f) the rms and peak current of each transistor. (g) Draw the waveform of fundamental load current and show the conduction intervals of transistors and diodes. Calculate the conduction time of (h) the transistors, and (i) the diodes.

Solution

$V_s = 220$ V, $f_0 = 60$ Hz, $R = 10\ \Omega$, $L = 31.5$ mH, $C = 112\ \mu$F, and $\omega = 2\pi \times 60 = 377$ rad/s. The inductive reactance for the *n*th harmonic voltage is

$$X_L = j_n\omega L = j2n\pi \times 60 \times 31.5 \times 10^{-3} = j11.87n\ \Omega$$

The capacitive reactance for the *n*th harmonic voltage is

$$X_c = -\frac{j}{n\omega C} = -\frac{j10^6}{2n\pi \times 60 \times 112} = \frac{-j23.68}{n}\ \Omega$$

The impedance for the *n*th harmonic voltage is

$$|Z_n| = \sqrt{R^2 + \left(n\omega L - \frac{1}{n\omega C}\right)^2} = [10^2 + (11.87n - 23.68/n)^2]^{1/2}$$

and the load impedance angle for the *n*th harmonic voltage is

$$\theta_n = \tan^{-1}\frac{11.87n - 23.68/n}{10} = \tan^{-1}\left(1.187n - \frac{2.368}{n}\right)$$

a. From Eq. (6.12), the instantaneous output voltage can be expressed as

$$v_o(t) = 280.1 \sin(377t) + 93.4 \sin(3 \times 377t) + 56.02 \sin(5 \times 377t) + 40.02 \sin(7 \times 377t) + 31.12 \sin(9 \times 377t) + \cdots$$

Dividing the output voltage by the load impedance and considering the appropriate delay due to the load impedance angles, we can obtain the instantaneous load current as

$$i_o(t) = 18.1 \sin(377t + 49.72°) + 3.17 \sin(3 \times 377t - 70.17°) + \sin(5 \times 377t - 79.63°) + 0.5 \sin(7 \times 377t - 82.85°) + 0.3 \sin(9 \times 377t - 84.52°) + \cdots$$

b. The peak fundamental load current is $I_{m1} = 18.1$ A. The rms load current at fundamental frequency is $I_{o1} = 18.1/\sqrt{2} = 12.8$ A.

c. Considering up to the ninth harmonic, the peak load current,

$$I_m = (18.1^2 + 3.17^2 + 1.0^2 + 0.5^2 + 0.3^2)^{1/2} = 18.41 \text{ A}$$

The rms harmonic load current is

$$I_h = (I_m^2 - I_{m1}^2)^{1/2} = \frac{18.41^2 - 18.1^2}{\sqrt{2}} = 2.3789 \text{ A}$$

Using Eq. (6.8), the THD of the load current,

$$\text{THD} = \frac{(I_m^2 - I_{m1}^2)^{1/2}}{I_{m1}} = \left[\left(\frac{18.41}{18.1}\right)^2 - 1\right]^{1/2} = 18.59\%$$

d. The rms load current is $I_o \approx I_m/\sqrt{2} = 18.41/\sqrt{2} = 13.02$ A, and the load power is $P_o = 13.02^2 \times 10 = 1695$ W. Using Eq. (6.5), the fundamental output power is

$$P_{o1} = I_{o1}^2 R = 12.8^2 \times 10 = 1638.4 \text{ W}$$

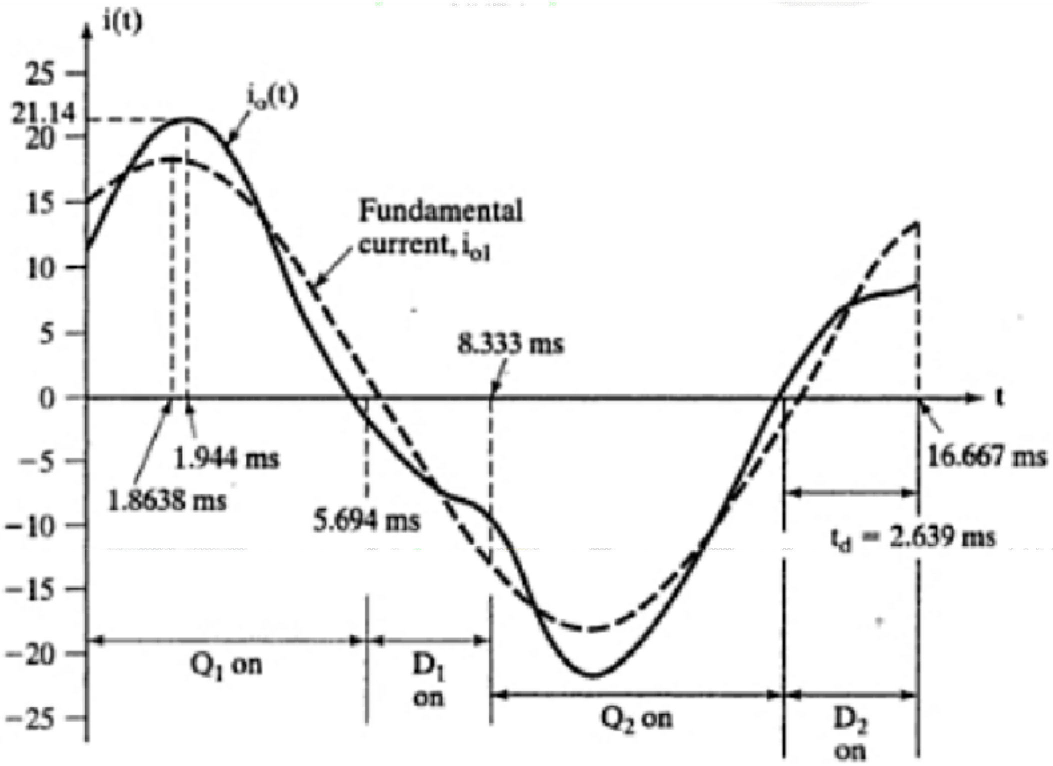


FIGURE 6.3

Waveforms for Example 6.3.

e. The average supply current $I_s = P_o/V_s = 1695/220 = 7.7$ A.

f. The peak transistor current $I_p \cong I_m = 18.41$ A. The maximum permissible rms current of each transistor is $I_{Q(\max)} = I_o/\sqrt{2} = I_p/2 = 18.41/2 = 9.2$ A.

g. The waveform for fundamental load current $i_1(t)$ is shown in Figure 6.3.

h. From Fig. (6.3), the conduction time of each transistor is found approximately from $\omega t_0 = 180 - 49.72 = 130.28°$ or $t_0 = 130.28 \times \pi/(180 \times 377) = 6031\ \mu s$.

i. The conduction time of each diode is approximately

$$t_d = (180 - 130.28) \times \frac{\pi}{180 \times 377} = 2302\ \mu s$$