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# Double-fin FETs based on standard CMOS approach

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ABSTRACT

Double-fin p-MOSFETs have been fabricated using PaDEOx process. SOI 133 nm wide and bulk 260 nm-wide FinFETs have been electrically characterized and compared with the photolithographically patterned 9 µm wide fin transistor based on the same layout. Extraction of device parameters: $g_M$, $V_T$, $SS$, $I_{D,off}$, $R_s$, $R_c$ has been done using sets of devices of different dimensions. The characterization results confirm advantages of double-fin devices.

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## 1. Introduction

Multi-gate MOS transistors (MuGFETs) exhibit a number of advantages as compared to their single-gate counterparts. The most pronounced feature is a strongly increased immunity to the short-channel effects (SCE). The gate, which wraps the MOSFET channel allows for better control over the channel formation and operation. A FinFET seems to be one of the most promising devices amongst the different types of MuGFETs [1]. Development of a cost-effective and efficient CMOS process for test FinFET manufacturing has been the aim of the work.

## 2. Device fabrication

Three types of MOSFETs, in which a transistor action occurs within a fin-type silicon path, have been fabricated. A general purpose CMOS test structure mask set has been used. The test structure layout has been designed using 3 µm critical dimension design rules.

A standard p-MOS transistor with modified surroundings of an active area is the first device. Dry etch of the active area pattern surroundings has resulted in lowering of the surface by 1.3 µm – Fig. 1a.

Next, a 28 nm thick gate oxide has been thermally grown and poly-Si gate has been deposited and patterned at two sidewalls and a top surface of a transistor fin – Fig. 2.

A commonly used LOCOS technique plays an important role in a fabrication process of the second variant of the FinFET-type devices. The LOCOS technique employs a nitride pattern as a mask against field oxidation to define MOSFET active areas. At the boundary of the nitride a so-called "birds beak" appears. It is thicker than the neighbouring plane field oxide layer. This subtle effect has been successfully used in a Pattern Definition by Edge Oxidation method (PaDEOx) [2] for fabrication of narrow silicon lines. According to this technique, after the field oxidation, the entire nitride layer and a most part of the oxide are carefully removed to reveal an oxide path along the "birds beak" region. The remaining oxide path serves as a mask in successive etching of a fin-shaped Si narrow path. The PaDEOx process has been considerably improved in this work. Width of the Si fin can be controlled in a wide range, down to approximately 20 nm. Dependence of the fin width on thickness of the oxide surrounding the nitride pattern and on the nitride layer thickness is shown in Fig. 3.

The PaDEOx process allows for one-dimensional scaling down of transistor channel width; other sizes of the device are subjected to lithography critical dimension limits in a standard way.

A pair of 0.26 µm wide and 0.67 µm high fins has been manufactured in order to create a double-fin p-MOS transistor – Fig. 1b. The same layout has been used and other fabrication details have been similar to those of the above-described wide fin device – Fig. 4.

The third transistor has been manufactured using SOI p-type wafers, which have been implanted with phosphorus ions to convert them to n-type. Double-fins have been prepared by means of PaDEOx technique. Next, the p-MOS FinFETs have been fabricated in a typical self-aligned process (Figs. 1c and 5).

All the presented devices have been passivated with PSG layer. Finally, Ti:W/Al metallization has been used.

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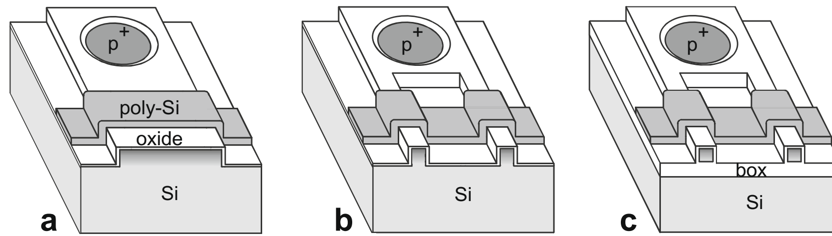


**Fig. 1.** Schemes of fabricated devices: (a) bulk MOSFET with a single wide fin; (b) double-fin bulk FET; and (c) double-fin SOI FET.

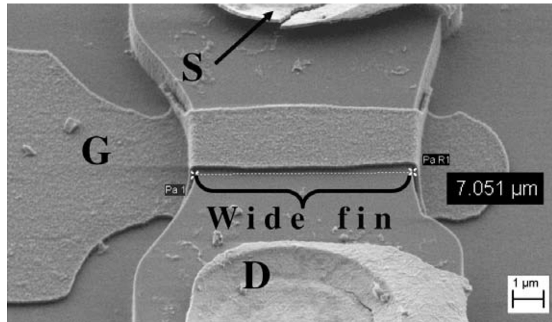


**Fig. 2.** SEM image of the HF-etched wide bulk FinFET.

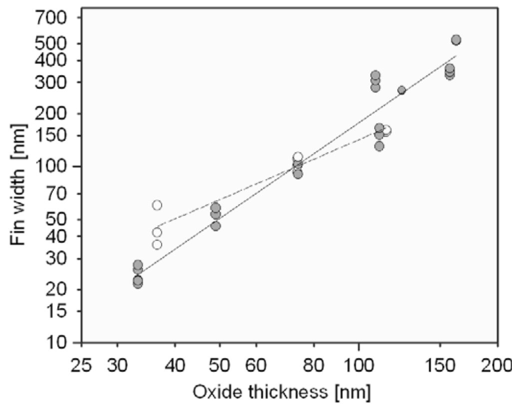


**Fig. 3.** Fin width versus oxide thickness for two nitride thicknesses: 64 nm – closed dots; 40 nm – open dots.

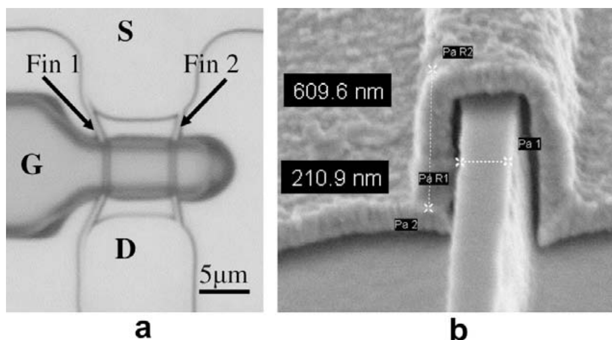


**Fig. 4.** (a) Top view of double-fin bulk FET and (b) SEM image of the individual fin after oxide etching.

## 3. Characterization of FinFETs

Drain current ($I_D$) versus gate and drain voltages ($V_{GS}$, $V_{DS}$) has been measured for series of FinFETs using a standard Keithley System 93 *I–V* setup. The test structure layout allows for evaluation of parameters of FinFETs with different fin lengths and different fin separations, determined by the widths of the MOSFET active areas – equal to channel widths in case of wide fin transistors (Fig. 1a).

### *3.1. Wide bulk FinFETs*

The wide bulk-type quasi-FinFETs (Figs. 1a and 2) exhibit a correct electrical behaviour. The basic electrical parameter values remain in reasonable ranges. Particularly, it is worthwhile to

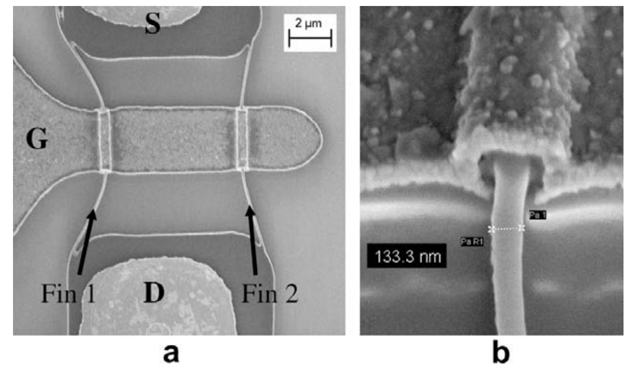


**Fig. 5.** SEM images: (a) top view of double-fin SOI FET and (b) the individual 133 nm wide and approximately 200 nm high fin – zoom in.

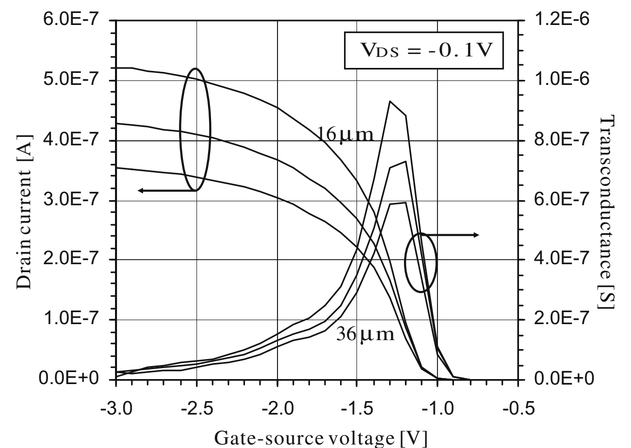


**Fig. 6.** $|I_D| - V_{GS}$ and $g_M - V_{GS}$ characteristics of series of wide bulk-type FinFETs; nominal fin width is 9 µm, fin height −1.3 µm, channel lengths are 16, 25, 36 µm.

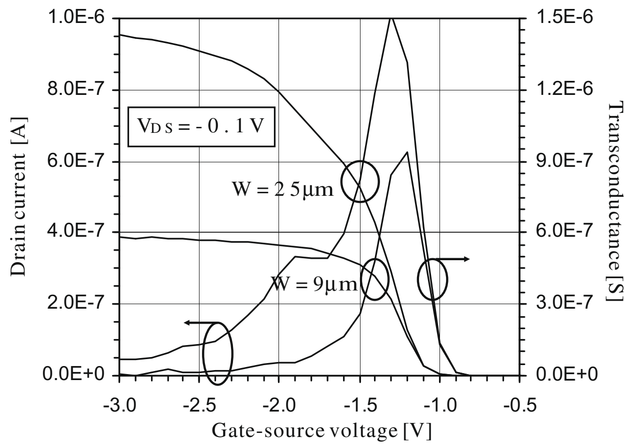


**Fig. 7.** $|I_D| - V_{GS}$ and $g_M - V_{GS}$ characteristics of series of wide bulk-type FinFETs; fin widths are 9, 25 μm, fin heights is 1.3 μm and the channel length is 9 μm.

mention a low value of the drain current in the off-range (7–12 pA) and a relatively low value of the subthreshold slope (about 80 mV/dec). The threshold voltage of these devices is about −1.05 V. The measurement results are shown in Fig. 6.

Nevertheless, the *I–V* characteristics of the wide FinFETs exhibit several undesired effects. Firstly, slight concavities at the $I_D - V_{GS}$ curves, and corresponding bends at the $g_M - V_{GS}$ curves may be stated just above the threshold. Probably different conduction paths are subsequently turned-on. They may be related to the top and side-wall surfaces of the wide fin (Fig. 7). A contribution of the bulk substrate also cannot be disregarded.

Secondly, a high degradation of *I–V* characteristics in the strong inversion range by the series resistance may be stated. It is manifested by a strong bowing of the $I_D - V_{GS}$ curves and by steep decrease of the $g_M - V_{GS}$ plots (Figs. 6 and 7). Tests of *p* + resistors have revealed a single contact resistance $R_c \approx 27.5$ kΩ. This, together with resistance of the source/drain diffusion areas leads to the *I–V* curves distortion.

### 3.2. Double-fin bulk FETs

Similarly to the wide fin device the double-fin ones (Figs. 1b and 4) exhibit correct electrical characteristics. The calculated values of the transconductance factor are of the order of $3.5–5.5 \times 10^{-6}$ A/V$^2$, the threshold voltage is in the range −1.1–−1.02 V, and the subthreshold slope is close to 150 mV/dec (Fig. 8). The drain current in the off-state is well below 10 pA. Moreover, due to a very similar method of contact formation as in the case of wide devices, the contact resistances are approximately the same as in the case of the wide MOSFETs.

As the devices with different fin separations exhibit very similar *I–V* characteristics, we may conclude that the current flows predominantly within the thin fins. In this context, and taking into account much better subthreshold behaviour of the wide devices, it is difficult to discover the real cause standing behind the relatively large value of the subthreshold swing.

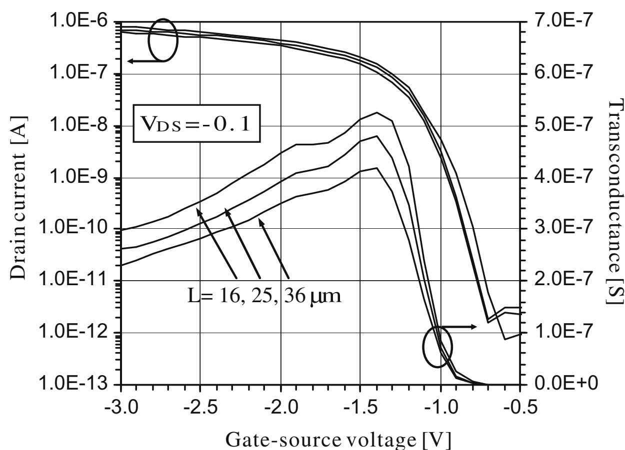


**Fig. 8.** $|I_D| - V_{GS}$ and $g_M - V_{GS}$ characteristics of series of bulk-type, narrow, double-fin FinFETs; fin separation is 9 μm, fin widths are 260 nm, channel lengths – 16, 25, 36 μm.

### 3.3. Double-fin SOI FETs

The measurements of the double-fin SOI FETs (Figs. 1c and 5) have revealed the following parameters: transconductance factor $1–1.5 \times 10^{-6}$ A/V$^2$, threshold voltage −2.15–−2.25 V, subthreshold slope 108–150 mV/dec, off-current $I_{D,off}$ below 10 pA (Figs. 9 and 10). It has appeared however, that the SOI-based devices suffer from large variations, which result from smaller dimensions and process spread.

Obviously, the perfect SOI insulation between fins makes the *I–V* characteristics independent on the fin separation.

### 3.4. Comparison of the FinFETs

Degradation of the $I_D - V_{GS}$ characteristics has been found. It is emphasized in $g_M - V_{GS}$ data. As has been mentioned above, it results from large series resistance, consisting of contact resistance and resistances of source/drain areas. For extraction of parasitic resistance a method [3] has been used. Accordingly $I_D - V_{GS}$ data of a series of MOSFETs with different nominal channel lengths L have been measured. Next, the measured drain-source resistances $R_m$ of these devices have been calculated using a formula (1).

$$R_m = \frac{V_{DS}}{I_D} = R_S + (L + \Delta L) \times f(P, V) \quad (1)$$

In Eq. (1) $R_S$ is a series resistance, while the rightmost term is a channel resistance, which may be expressed as a product of effective channel length $L_{eff} = L + \Delta L$, and a function $f(P, V)$ dependent on device parameters and terminal voltages. Next, a linear regression has been applied to (1) for a number of the gate-source voltages. However, the resulting lines do not have a single cross-section

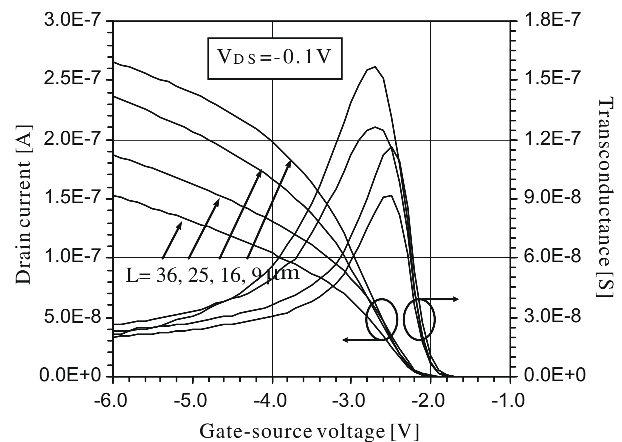


**Fig. 9.** $|I_D| - V_{GS}$ and $g_M - V_{GS}$ characteristics of series of SOI double-fin FinFETs; fin separation is 9 μm, fin widths are 133 nm, channel lengths – 9, 16, 25, 36 μm.

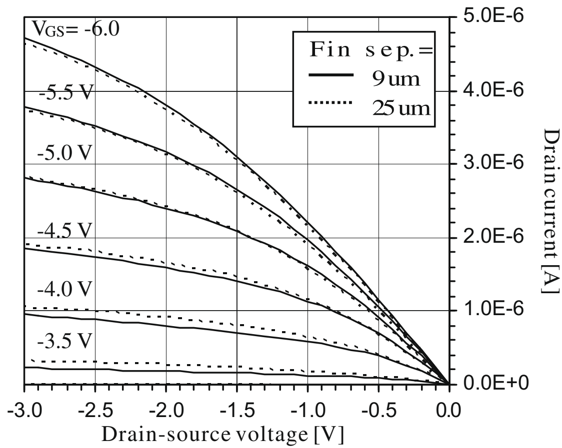


**Fig. 10.** $|I_D| - V_{DS}$ characteristics of series of SOI, double-fin FinFETs; nominal channel length is 9 μm, fin widths are 133 nm, fin separations – 9, 25 μm.

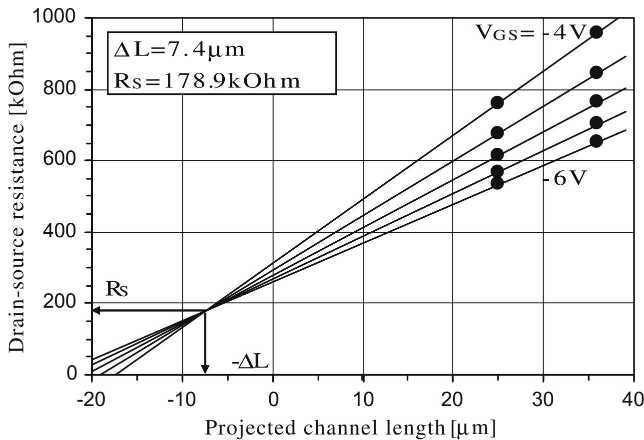


**Fig. 11.** Extraction of series resistance and effective channel length for double-fin SOI FinFETs (fin widths are 133 nm, fin heights – 200 nm, channel lengths – 16, 25, 36 μm, fin separation – 9 μm).

point at ($-\Delta L$, $R_S$) point, as expected based on (1). So, additional linear regression between coefficients $A$ and $B$ of Eq. (2) resulting directly from (1) has been used [3].

$$R_m = A \times L + B; B = A \times \Delta L + R_S \quad (2)$$

This method has been used for three types of devices. The $R_S$ values are as follows: 21 kΩ (wide bulk quasi-FinFETs), 51 kΩ (narrow bulk FinFETs), 179 kΩ (narrow SOI FinFETs). Although these results are not fully consistent with the contact resistances obtained using the resistor measurements, the trend between structures is similar. The differences between results may be attributed to a spread of transistor dimensions and of contact formation process. The data processing for SOI FinFETs is shown in Fig. 11. The contact resistance values seem to be very high, hence the further work will be focused on their improvement.

The calculated transconductances of the three fin variants have been normalized against the effective device operation area. The results may be summarized as follows: wide bulk quasi-FinFETs – $0.56 \times 10^{-6}$ AV$^{-2}$ μm$^{-2}$, double-fin bulk FinFETs – $13.7 \times 10^{-6}$ AV$^{-2}$ μm$^{-2}$, and double-fin SOI FinFETs – $39.8 \times 10^{-6}$ AV$^{-2}$ μm$^{-2}$. This confirms advantages of FinFETs in terms of current load under given gate control conditions.

## 4. Conclusions

Two variants of test FinFETs with 133 nm and 260 nm-wide fins, together with a reference wide quasi-FinFET have been successfully fabricated. They have been prepared by means of a standard photolithography process of 3 μm critical dimension. The electrical characteristics of the devices, though non-ideal, exhibit correct device behaviour. The parameters, e.g. threshold voltage, off-current have satisfactory values. Moreover, it has been shown, that the narrow fin devices sustain a significantly higher current load density, than the wide ones.

Device sizes have been matched to requirements of the CMOS process, which is a basic Si technology used in the IET lab. Nevertheless, fabrication of transistors with channel width narrower more than 20 times than critical dimension limit of the used lithography technique certifies advantages of the PaDEOx process. One-dimensional scaling of Si lines down to 20 nm region seems to be realistic with use of even more than hundred nm fabrication plants. More aggressive scaling needs solution of problem of fin side-wall roughness and related issues.

The proposed CMOS-compatible process is expected to be a cost-effective method for fabrication of the FinFETs and other narrow Si wire-based devices, which may be used in CMOS and sensor applications.

## Acknowledgements

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