This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

Optimal Low Switching Frequency Pulsewidth Modulation of Nine-Level Cascade Inverter

Amarendra Edpuganti, *Student Member, IEEE* and Akshay K. Rathore, *Senior Member, IEEE*

***Abstract*—Synchronous optimal pulsewidth modulation (SOP) permits low switching frequency modulation of multilevel inverter for medium-voltage high-power industrial AC drives without compromising on total harmonic distortion (THD). An aim of our experiment was to operate nine-level cascade inverter of an induction motor drive at an average device switching frequency limited to rated fundamental frequency by using SOP technique. To reduce the number of separate DC sources, a three-level diode clamped converter was used as a cell in a nine-level cascade inverter. Using SOP technique, optimal nine-level waveforms were obtained by off-line optimization assuming steady-state operation of the induction machine. The switching angles for each semiconductor switch are then obtained from optimal nine-level waveforms based on the criteria to minimize the switching frequency as well as unbalance in DC-link capacitor voltages. Experimental results obtained from the 1.5 kW induction motor drive show THD $< 5\%$ for stator currents. The results indicate that SOP technique reduces the switching frequency of operation without compromising on THD.**

***Index Terms*—Synchronous optimal pulsewidth modulation, Low switching frequency modulation, Multilevel inverters, Medium-voltage AC drives.**

I. Introduction

MULTILEVEL converters are now well-established and standard solution for medium and high voltage high power applications and power-quality demanding solutions. The advantages of multilevel converters over two-level converters are higher voltage operating capability with medium voltage semiconductor devices, improved output voltages with less harmonic distortion, lower common-mode voltages, less $\frac{dv}{dt}$ stress, near sinusoidal input currents, smaller input and output filters, increased efficiency due to possibility of low switching operation, reduced electromagnetic interference (EMI) problems and possible fault-tolerant operation [1]–[9]. In addition, the torque ripple also reduces as number of levels increases in case of multilevel inverter fed AC drives. In high power applications, the switching losses contribute to major portion of total device losses and thus low switching frequency operation is necessary to achieve higher efficiency. However, minimizing switching frequency increases the harmonic distortion. Therefore, the challenge is to minimize the harmonic distortion while reducing the switching frequency.

Presently, the most popular topologies are diode-clamped or neutral-point-clamped (NPC), capacitor-clamped or flying capacitor (FC) and cascaded H-Bridge (CHB) [3]. The CHB topologies are preferred for higher-level converters due to requirement of least number of components and ease of control compared to other topologies. In addition, modularized circuit layout and packaging is also possible with CHB topology because each level has similar structure [10]. However, one major drawback of this topology is requirement of multiple numbers of DC-sources, which is not feasible in many applications. One of the method for reducing the number of DC sources is to replace H-Bridge cell with NPC or FC converters [11]. However, an important issue with the topologies having NPC or FC converters is voltage unbalance of DC-link capacitors that further adds to harmonic distortion of output voltage waveforms. An auxiliary capacitor-based balancing approach has been proposed to equalize the DC-link capacitor voltages for NPC five-level converter [12].

Several low switching frequency modulation techniques have been proposed for high power applications. A new modulation method for modular multilevel converter operating at fundamental switching frequency while successfully eliminating fifth harmonic was proposed in [13]. A novel switching sequence design for the space-vector modulation (SVM) of high-power multilevel converters optimized for the improvement of harmonic spectrum and the minimization of device switching frequency was proposed in [14]. A new control method for seven-level cascaded inverter operating at fundamental switching frequency was proposed by Zhong Du et al. [15]. Model predictive current control algorithm has been demonstrated for CHB nine-level inverter with switching frequency between 425 Hz to 500 Hz [16]. Also, an adaptive duty-cycle modulation algorithm that reduces the switching frequency by using the slope of the voltage reference to adapt the modulation period was proposed by Kouro et al. [17]. By using this method the switching frequency of operation has been maintained between 285 Hz to 785 Hz for nine-level asymmetric CHB inverter.

The selective harmonic elimination (SHE) method is one of the low-switching frequency control technique which eliminates $(n-1)$ lower order harmonic components, n being the number of switching angles. Generalized SHE technique in Fourier domain for two-level single phase and three phase inverters has been proposed by patel et al.[18]−[19]. Programmed PWM technique for minimizing the harmonics has been reported [20]−[21]. A new method for SHE based on six-step symmetry [22] and by use of Walsh functions to obtain Fourier spectral equations has been reported [23]−[24]. A new solution to convert the transcendental equations into polynomial equations for SHE has been proposed [25]. The general problem formulation and selected solutions for both unipolar and bipolar switching patterns to eliminate the fifth and seventh harmonics are presented by Wells et al. [26]. A

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

novel method to achieve fast transient response and efficient harmonic (disturbance) filtering has been achieved by using signal processing methods [27]. A minimization method to derive multiple sets of solutions for the bipolar SHE PWM method for both single-phase and three-phase converters has been presented in [28]. A real-time SHE method by using modified triangle carrier has been proposed instead of conventional offline solution of switching angles [29]. In this method, initial guess is not required as well as switching frequency is not restricted to integer multiple of fundamental frequency [30]. SHE is also extended for multilevel converters. A unified approach to solving the harmonic elimination equations in multilevel converter to obtain the switching angles in the lower range of modulation indices has been reported [31]. A Bee algorithm (BA) for SHE has been reported by Kavousi et al. for cascaded multilevel inverter [32].

Synchronous optimal pulsewidth modulation (SOP) technique is an emerging technology to reduce switching frequency without compromising on harmonic distortion. Unlike SHE method, SOP takes into account all possible lower order harmonic components and determines switching angles so as to keep the THD of output voltage or current waveforms within limits. SOP consists of Fourier series analysis of output voltage or current waveforms to model equations using switching angles as variables and their optimization to reduce THD. All the calculations are computed off-line assuming steady state operating conditions. Hence, this method is only suitable for low performance drives such as centrifugal pumps, industrial fans, blowers etc which operate in open-loop ($\frac{v}{f}$) control mode. In steady-state operating conditions, SOP method for controlling five-level inverters [33]−[34] and dual three-level inverters [35]−[36] with maximum switching frequency of 200 Hz have been demonstrated. In case of high performance drives which are subjected to frequent transient conditions, using traditional closed-loop control techniques with SOP technique intervenes with optimal switching patterns and hence, a real-time optimization is required. Thus, initially optimal stator current trajectory tracking method has been proposed [37]−[38]. Then, trajectory of optimal stator flux vector which is independent of machine parameters or load conditions has been suggested as tracking agent [39]–[42]. Nonetheless, the application of SOP has not been reported for multilevel inverters with more than five-levels. Therefore, the objective of the present study is to demonstrate SOP technique for operating nine-level cascade inverter of induction motor drive at an average device switching frequency limited to rated fundamental frequency (50 Hz) in open loop ($\frac{v}{f}$) control mode. It should be pointed out that proposed SOP technique can be used for any nine-level inverter topology by modifying the method of assigning switching angles for each power semiconductor switch based on optimal nine-level waveforms.

Cascaded nine-level inverter topology and its steady-state operation are discussed in section II, analysis of SOP for nine-level inverter is explained in section III, realization of optimal nine-level waveforms at low device switching frequency is discussed in section IV. Experimental results are demonstrated in section V to show the effectiveness of the proposed modulation.

II. Nine-Level Cascade Inverter

The nine-level cascade inverter topology is shown in Fig. 1. It has two H-bridges connected in series that have NPC converters in each leg. The output of each H-Bridge contains five-levels and thus it is possible to obtain nine-level waveforms in each phase. Each phase requires two DC power sources. The output of inverter is directly connected to induction motor without a LC filter in our case.

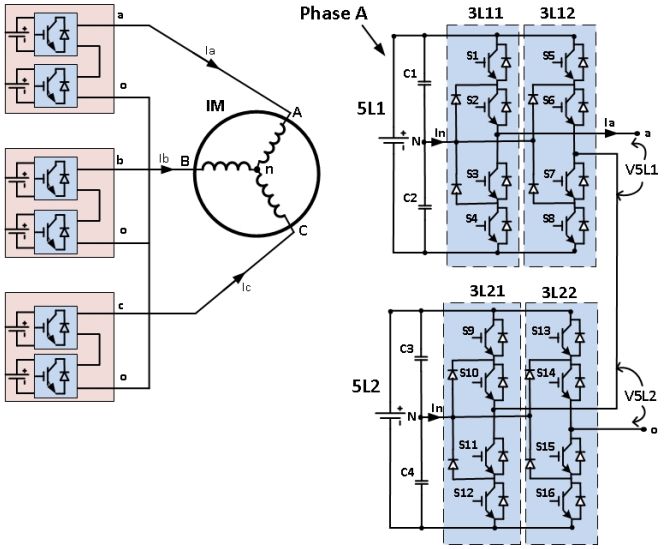


Fig. 1. Nine-level cascade inverter

Table I: Operation of nine-level inverter

$\mathbf{V_{9L}}$	$\mathbf{V_{5L1}}$	$\mathbf{V_{3L11}}$	$\mathbf{V_{3L12}}$	$\mathbf{V_{5L2}}$	$\mathbf{V_{3L21}}$	$\mathbf{V_{3L22}}$
-4V_{dc}	-2V_{dc}	$-V_{dc}$	V_{dc}	-2V_{dc}	$-V_{dc}$	V_{dc}
$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	0
	-V_{dc}	$-V_{dc}$	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
-2V_{dc}	-2V_{dc}	$-V_{dc}$	V_{dc}	0	0	0
	-V_{dc}	$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	0
	0	0	0	-2V_{dc}	$-V_{dc}$	V_{dc}
-V_{dc}	-2V_{dc}	$-V_{dc}$	V_{dc}	V_{dc}	V_{dc}	0
	-V_{dc}	$-V_{dc}$	0	0	0	0
	0	0	0	$-V_{dc}$	$-V_{dc}$	0
	V_{dc}	V_{dc}	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
0	0	0	0	0	0	0
V_{dc}	-V_{dc}	$-V_{dc}$	0	2V_{dc}	V_{dc}	$-V_{dc}$
	0	0	0	V_{dc}	V_{dc}	0
	V_{dc}	V_{dc}	0	0	0	0
	2V_{dc}	V_{dc}	-V_{dc}	-V_{dc}	$-V_{dc}$	0
2V_{dc}	0	0	0	2V_{dc}	V_{dc}	-V_{dc}
	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}	0
	2V_{dc}	V_{dc}	-V_{dc}	0	0	0
3V_{dc}	V_{dc}	V_{dc}	0	2V_{dc}	V_{dc}	-V_{dc}
	2V_{dc}	V_{dc}	-V_{dc}	V_{dc}	V_{dc}	0
4V_{dc}	2V_{dc}	V_{dc}	-V_{dc}	2V_{dc}	V_{dc}	-V_{dc}

In each H-Bridge, the NPC converters generate three voltage levels $(-V_{dc}, 0, V_{dc})$ with respect to neutral point of DC-link capacitors 'N' and thus a five voltage levels

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

$(-2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc})$ are obtained at the output terminals of each H-Bridge. By connecting two H-Bridges in series, it is possible to obtain nine level output voltage waveform $(-4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc})$ in each phase. The operation of nine-level inverter is explained in Table I.

III. Synchronous Optimal Pulsewidth Modulation (SOP)

SOP generates optimal switching pulse patterns of semiconductor devices in a multilevel inverter [43]. Synchronized PWM is used in low switching frequency applications where carrier signal at frequency (f_s) and sinusoidal control signal at frequency (f_1) are synchronized with each other i.e. $\frac{f_s}{f_1}$ is an integer in order to eliminate sub-harmonic frequencies which are undesirable in many applications. Synchronized PWM results in lower number of switching instants per fundamental period and even a little variation in these switching angle values will have considerable influence on the harmonic distortion of output voltage [44]. Optimization methods are suggested to pre-determine switching angles off-line to reduce harmonic distortion [45]. The pre-calculated switching angles are stored and retrieved during real-time operation.

A. Mathematical Analysis

Consider a typical nine-level output phase voltage waveform $(v_{jo}, j = a, b, c)$ shown in Fig. 2 with switching angles at $\alpha_1, \alpha_2, \alpha_3, \alpha_4$ in a quarter period. By introducing half-wave and quarter-wave symmetry in the switching pattern eliminates all even harmonics. Using Fourier series analysis, harmonic components of v_{jo} are obtained as,

$$u_k = \frac{V_{peak}}{k\pi} \sum_{i=1}^{N} s(i) cos(k\alpha_i) \tag{1}$$

where, V_{peak} represents the peak value of voltage waveform which is equal to $4V_{dc}$, k corresponds to *kth* harmonic (*k*=1,3,5,7....), u_k is the amplitude of *kth* harmonic voltage component of v_{ko} and *s(i)* represents the slopes of switching transitions at switching angles α_i which is equal to 1 when switching to higher potential and -1 when switching to lower potential. It should be noted that dc-link voltages (V_{dc}) are assumed constant [33-34,36] while deriving (1). This assumption holds true for H-bridge based multilevel topologies whereas for 3L-NPC phase leg based topologies additional control measures are required [46].

The phase voltages applied to induction motor are given by $v_{jn} = v_{jo} - v_{no}$ (j=a,b,c). The waveform v_{no} contain all the triplen harmonics of v_{jo} with amplitude equal to one third of amplitude of v_{jo}. So, phase voltage v_{jn} has other harmonics of v_{jo} except triplen harmonics [44]. Assuming that stator currents are determined by leakage inductances, the expressions for harmonic components of stator current i_k and harmonic rms current i_h is given by,

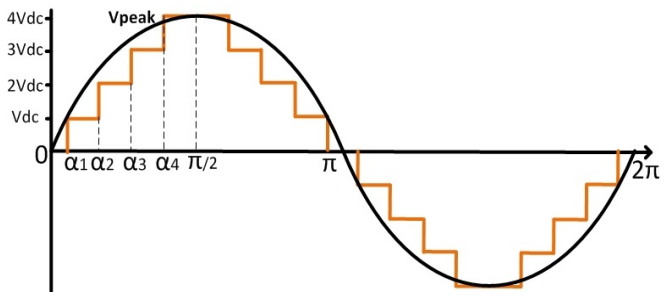


Fig. 2. Nine-level Voltage Waveform

$$i_k = \frac{u_k}{\omega_1 l_\sigma k} = \frac{V_{peak}}{\omega_1 k^2 l_\sigma \pi} \left(\sum_{i=1}^{N} s(i) cos(k\alpha_i) \right) \tag{2}$$

$$i_h = \sqrt{\sum_k i_k^2} = \frac{1}{\omega_1 l_\sigma} \sqrt{\sum_k \left(\frac{u_k}{k}\right)^2} \tag{3}$$

where, w_1 is the fundamental frequency of stator, l_σ is the leakage inductance of the machine and *k* corresponds to odd order harmonics (*k*=5,7,11,13...).

In SOP, the switching angles are optimized in order to reduce the harmonic distortion. In order to eliminate the influence of leakage inductance in optimization function, distortion factor (DF) is used as a figure of merit [44]. The expression for DF is obtained as,

$$d = \frac{i_h}{i_{h,six-step}} \tag{4}$$

where, i_h, $i_{h,six-step}$ represents the harmonic rms current during normal operation and six step operation (m=1 or at rated fundamental frequency) of multilevel inverter respectively. For six-step operation, the expressions for $u_{k,six-step}$ and $i_{k,six-step}$ are obtained as,

$$u_{k,six-step} = \frac{4V_{peak}}{k\pi} \tag{5}$$

$$i_{h,six-step} = \sqrt{\sum_k i_{k,six-step}^2} = \frac{1}{\omega_1 l_\sigma} \sqrt{\sum_k \left(\frac{u_{k,six-step}}{k}\right)^2}. \tag{6}$$

After simplifying (2)-(6), the final expression for DF is obtained as,

$$d = \frac{\sqrt{\sum_k (\frac{1}{k^4})(\sum_{i=1}^{N} s(i) cos(k\alpha_i))^2}}{4\sqrt{\sum_k (\frac{1}{k^4})}}. \tag{7}$$

It is obvious from (7) that DF depends on the two variables: switching transitions *s(i)* and switching angles α_i (*i*=1,2...*N*). It should be noted that, only a few certain combinations of switching transitions lead to nine-level waveforms. Therefore, the optimization problem is divided into three parts: (1) obtain all the possible switching transitions to obtain nine-level waveforms; (2) calculate the optimized switching patterns for each nine-level waveform in order to minimize DF; (3) select the structure that has least DF.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

B. Nine-level Structures

Depending on the switching transitions, multilevel inverter generates different structures of nine-level waveforms. A three-level converter has only one structure possible for a given number of switching angles, whereas five or higher-level converters have more number of structures due to additional degree of freedom of step transition to higher level. Fig. 3 shows the different possible structures for three and nine-level waveforms with twelve switching angles in half period.

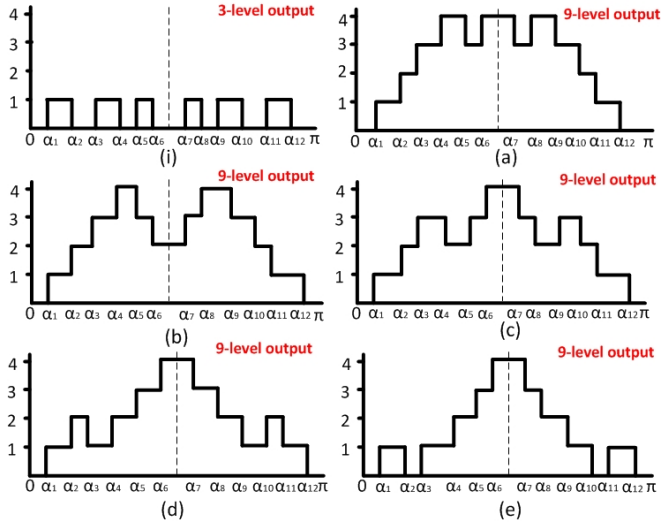


Fig. 3. Possible structures of three and nine-level waveforms

The number of switching angles over a quarter of fundamental period is known as pulse number (*N*). To obtain a nine-level waveform, minimum value of *N* should be equal to four and as value of *N* increases, the number of valid structures also increases. Table II shows the number of possible structures for a three, five and nine-level waveforms with pulse number *N* varying from 4 to 15. It is concluded that as number of levels increase, the number of valid structures increases rapidly as pulse number *N* increases.

Table II: Number of structures for three, five and nine-level waveforms

	Pulse Number *N*											
Level	4	5	6	7	8	9	10	11	12	13	14	15
3-Level	1	1	1	1	1	1	1	1	1	1	1	1
5-Level	3	3	7	7	15	15	31	31	63	63	127	127
9-Level	1	1	5	6	20	26	73	99	253	352	848	1200

C. Inverter Control

SOP technique requires optimal switching patterns to be calculated off-line for all steady-state operating points assuming constant $(\frac{v}{f})$ control. It is possible to use SOP technique for high dynamic performance requirement applications by combining with trajectory control method [41]−[42]. The modulation index (m) is defined as $\frac{f_1}{f_{1R}}$, where f_{1R} is the rated fundamental frequency of operation (50 Hz) and f_1 is the variable fundamental frequency of input voltage applied to induction motor. The relationship between pulse number *N* and f_1 is obtained as [33]

$$N = floor\left(\frac{4f_{smax}}{f_1}\right) = floor\left(\frac{4f_{smax}}{mf_{1R}}\right) \tag{8}$$

where, $f_{s,max}$ is the desired maximum switching frequency that is limited to a fixed value. Since the induction motor is operated at constant $(\frac{v}{f})$ control mode, one obtains

$$\frac{f_1}{f_{1R}} = \frac{u_1}{u_{1,six-step}}$$
$$4m = \sum_{i=1}^{N} s(i)\cos(\alpha_i). \tag{9}$$

Thus, (9) gives the constraint on switching angles to set the fundamental frequency of inverter output voltage waveform to f_1.

From (8), it should be observed that value of pulse number *N* is higher for low modulation index values, which leads to more number of possible structures. Consequently, the computation time to optimize all structures increases at lower modulation index values. In addition, performance of optimization reduces at lower modulation index values ($0 \leq m < 0.3$). Therefore, space vector modulation (SVM) is preferred for the lower modulation index values [36]−[37]. Moreover, high-power drives are designed to operate with high modulation index values ($m > 0.5$) [17] and hence, SOP method is best suited for these applications. In case of nine-level inverter, SOP technique is used for pulse numbers $N \leq 13$.

The signal flow graph in Fig. 4 explains the details of control algorithm. The magnitude of the reference voltage vector u_{ref} is used for selecting the optimal nine-level pattern P(m,N) which consists of optimized switching angles along with switching transitions $s(i)$. The optimal nine-level pattern p(m,N), phase angle of reference voltage vector and fundamental frequency (f_1) are given as input to modulator which generates nine-level switching state vector ${u_k}^{(9L)}$. The pattern generator divides the nine-level switching state sequence into four three-level switching state vectors $({u_{k1,2,3,4}}^{(3L)})$ for each phase of induction motor drive. The mechanism of pattern generator will be explained in section IV. It should be noted that the proposed algorithm can be applied for any nine-level inverter topology by modifying the mechanism of pattern generator. For example, if nine-level inverter consists of four H-Bridges connected in series then pattern generator should be modified to generate four switching state vectors $({u_{k1,2,3,4}}^{(HB)})$ for each phase.

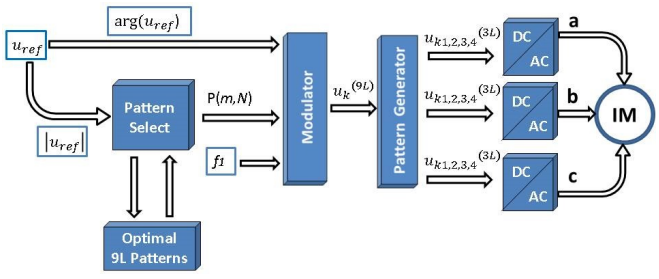


Fig. 4. Signal flow graph of nine-level inverter control algorithm

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

D. Optimization method

The goal of optimization is to generate optimal switching patterns for each steady state operating point (*m,N*) in order to minimize DF. The flowchart of optimization algorithm is shown in Fig. 5. The constraints of optimization are as follows [33]:

1) Sufficient gap (10μs) between consecutive switching angles to allow for minimum on times and off times of the power semiconductor devices.
2) In order to maintain current modulation index value, it is mandatory to satisfy the relation (9).
3) Continuity of switching angles for a given pulse number over its associated modulation index range in order to avoid transients in machine currents.

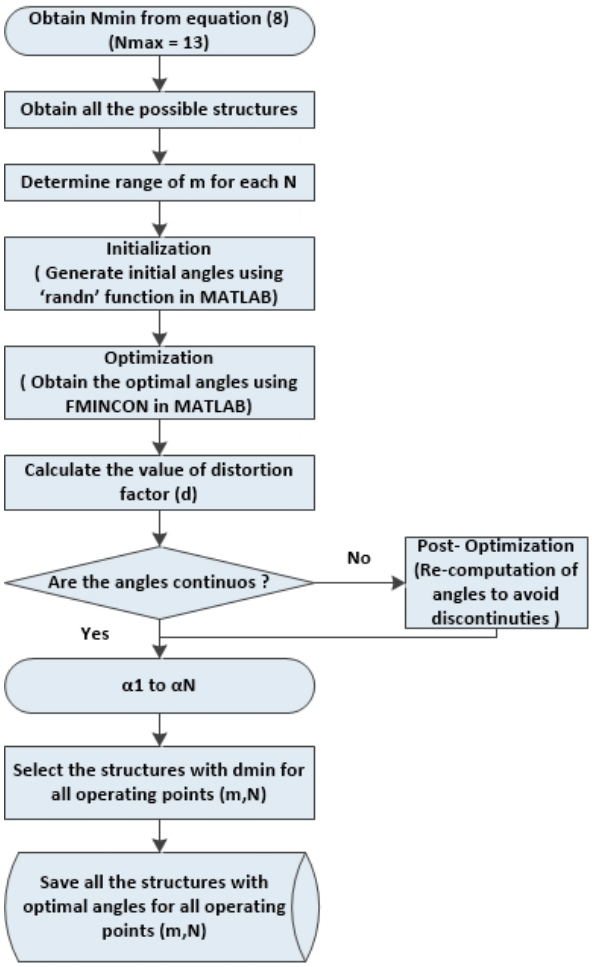


Fig. 5. Flowchart for optimization algorithm for nine-level inverter

In the beginning, all the possible structures for *N*= 4 to 13 are obtained in the form of switching transitions *s(i)*. For each pulse number *N*, modulation index range is determined and then for each operating point (*m,N*), MATLAB function "randn" is used to generate the initial values of switching angles for further optimization while satisfying the relation (9). The gradient method 'FMINCON', a built-in function in MATLAB is used for obtaining optimized switching patterns for each operating point (*m,N*). For DF calculations, only harmonic components up to 100 are considered. The optimization loop runs for all possible structures corresponding to each operating point (*m,N*) and then structure with least DF along with optimized pattern is recorded.

If switching angles for consecutive modulation index values differ by more than 5 degrees, post optimization is performed starting with optimized switching angles as initial values. Due to post-optimization, transients in machine currents will be avoided but the distortion factor will be slightly compromised. All the steps are repeated for *N*= 4 to 13. The final optimal switching angles are stored as complete patterns P(*m, N*) in a FPGA and they are retrieved during real time operation depending on the input voltage applied to induction motor.

E. Optimization Results

SOP technique is used for generating optimized switching patterns for nine-level inverter operating at maximum switching frequency of $f_{s,max}$ = 50 Hz. Fig. 6 shows the distortion factors for nine-level inverter before and after post optimization. When modulation index value becomes closer to unity, operation of converter will be similar to six-step operation that leads towards unity DF.

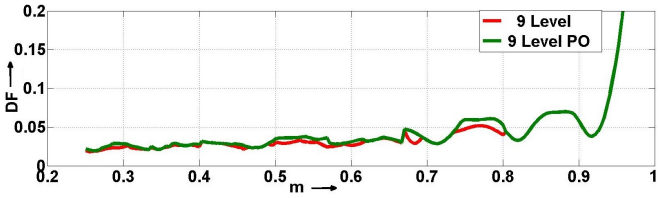


Fig. 6. DF for nine-level inverters operating at $f_{s,max}$=50 Hz

IV. Realization of Optimal Nine-Level Waveforms

One of the important steps after obtaining the optimal nine-level waveforms is assigning switching angles for each semiconductor device. As shown in Table I, optimal nine-level waveform is obtained by combining two five-level waveforms and each five-level waveform is obtained from two NPC legs of each H-Bridge. The challenge is to choose those combinations that reduce the maximum device switching frequency of semiconductor devices as well as minimize the voltage unbalance across DC-link capacitors of each H-Bridge.

A. Minimization of Unbalance in DC-link Capacitor Voltages

During optimization, dc-link voltages are assumed constant. In practice, it is important to reduce unbalance in DC-link voltages to avoid further distortion of machine currents and as well as to reduce the high voltage stress on power semiconductor devices as well as DC-link capacitors. As shown in Fig. 1, potential of neutral point 'N' is floating as dc-link voltages are not stabilized by external sources. The neutral point voltage changes in proportion to integral of neutral point current I_n. The neutral point current I_n depends on the load condition as well as switching patterns [47]. The difference between two DC-link capacitor voltages is termed as neutral point potential(NPP) error. As shown in Table III, charging and discharging of DC-link capacitors happens when the output potential of H-bridge is $\pm V_{dc}$, whereas if

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

the output voltage of H-bridge is 0 or $\pm 2V_{dc}$ then DC-link capacitor voltages remain constant. Due to natural balancing mechanism of NPC converters [48], the average value of NPP error tends to become zero in steady-state operating conditions and thus further distortion of machine currents is negligible. However, in case of transient operations as well as due to unequal switching patterns the NPP error might get accumulated and then average value of NPP error will not be zero. In the literature, several NPP balancing algorithms have been suggested to solve this problem [12,46-48].

Table III: Analysis of DC-link capacitor voltages of H-Bridge

5L	3L1	3L2	In	Vdc1	Vdc2
$2V_{dc}$	V_{dc}	$-V_{dc}$	0	Constant	Constant
V_{dc}	0	$-V_{dc}$	+ve	Charging	Discharging
V_{dc}	V_{dc}	0	-ve	Discharging	Charging
0	0	0	0	Constant	Constant
$-V_{dc}$	0	V_{dc}	-ve	Discharging	Charging
$-V_{dc}$	$-V_{dc}$	0	+ve	Charging	Discharging
$-2V_{dc}$	$-V_{dc}$	V_{dc}	0	Constant	Constant

Moreover, the ripple in DC-link capacitor voltages should be minimized otherwise it leads to high voltage stress on the power semiconductor devices and capacitors. This is possible by dividing the optimal nine-level waveform such that output potential of V_{5L1}, V_{5L2} is $\pm V_{dc}$ for shorter duration. For example, Fig. 7 demonstrates four possible realizations of a nine-level waveform and for combination(d), output potentials of V_{5L1}, V_{5L2} have voltage of V_{dc} for shorter time interval. Therefore, combinations (d) is preferable because it will lead to less unbalance in DC-link capacitor voltages compared to (a),(b) or (c). The exact value of unbalance depends on the load conditions.

B. Minimization of Switching Frequency of Semiconductor Devices

One more important criteria while assigning switching angles is to minimize the maximum device switching frequency of each semiconductor device. The pulse number *N* determines the number of switching transitions of the nine-level potential and each transition is being caused by a transition in one of four three-level NPC inverters. The total number of switching transitions in turn decides the switching frequency of semiconductor device, so the pulse number should be divided equally among all the four three-level inverters. However, even distribution of switching transitions among all four three-level inverters is possible only when *N* is a multiple of 4 otherwise splitting of switching transitions is not equal among each three-level inverter. Table IV shows such relevant possible division of pulse number *N* varying from 4 to 13, with last column corresponding to maximum value of average device switching frequency ($f_{s,avg}$). It should be observed that for *N*=4, 6 or 8, switching transitions are equally divided among all four three-level inverters, whereas for other values each three-level inverter will have different switching transitions. In addition, due to constraint of minimizing the DC-link voltage unbalance, equal division of switching transitions may not be possible even if *N* is a multiple of 4. This leads to three-level inverters operating at different switching frequencies and hence, different switching losses. However, it should be observed that average device switching frequency of nine-level inverter for any pulse number *N* is limited to rated fundamental frequency (50 Hz) as shown in Table IV. Additional measures like swapping of pulse sequences among four three-level NPC inverters is required to establish same number of switching transitions for all three-level NPC inverters and hence, same switching losses [36].

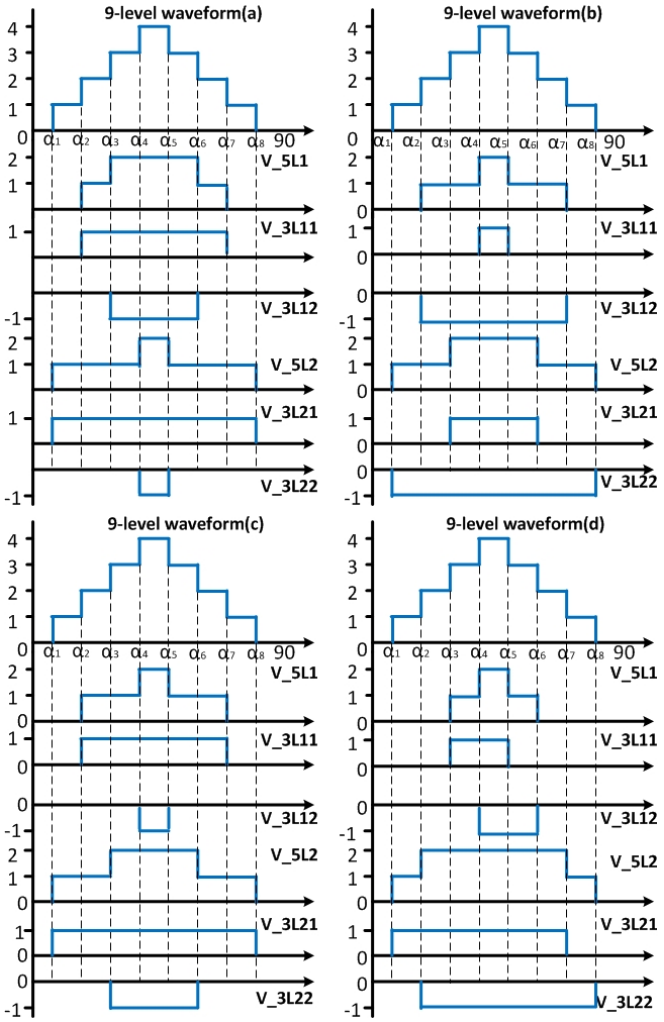


Fig. 7. Realization of Nine-level waveform

V. Experimental Results

The proposed SOP technique has been implemented for controlling a nine-level cascade inverter feeding a 1.5 kW induction motor . The experimental setup of nine-level cascade inverter for a single phase is shown in Fig. 8. Each leg of H-bridge was implemented by using 3-level NPC modules from Infineon and a six-pack IGBT driver SKHI 61R from Semikron was used as a driver. It should be noted that by using proper configuration pins it is possible to use SKHI 61R for driving three-level modules. The switching signals

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

Table IV: Division of pulse number N for nine-level inverter

N	$f_1(Hz)$	$5L1$	$3L1$	$3L2$	$5L2$	$3L3$	$3L4$	$f_{s,max}(3L1-3L4)(Hz)$	$f_{s,avg}(Hz)$
4	40.01-50	2	1	1	2	1	1	50, 50, 50, 50	50
5	33.34-40	2	1	1	3	1	2	40, 40, 40, 80	50
6	28.57-33.33	3	1	2	3	1	2	33.33, 66.67, 33.33, 66.67	50
7	25.01-28.56	3	2	1	4	2	2	57.14, 28.57, 57.14, 57.14	50
8	22.22-25	4	2	2	4	2	2	50, 50, 50, 50	50
9	20.01-22.21	4	2	2	5	2	3	44.44, 44.44, 44.44, 66.66	50
10	18.19-20	5	2	3	5	3	2	40, 60, 60, 40	50
11	16.68-18.18	5	2	3	6	3	3	36.36, 54.54, 54.54, 36.36	50
		5	3	2	6	2	4	54.54, 36.36, 36.36, 72.72	
12	15.39-16.67	6	3	3	6	3	3	50, 50, 50, 50	50
13	14.29-15.38	6	3	3	7	3	4	46.15, 46.15, 46.15, 61.52	50

were programmed on a Xilinx Spartan-6 FPGA. The induction motor was supplied with phase voltage of 110 V at rated fundamental frequency (50 Hz) and thus the DC-link capacitor voltages were obtained as 30.56 V and input voltages to H-Bridge were obtained as 61.12 V from (5). Table V shows the list of major components along with their parameters.

Fig. 8. Single phase of a nine-level cascade converter

Table V: Parameters of major components in experimental setup

Components	Parameters
Induction Motor	1.5 kW, 400 V, 50 Hz
3-level Module	F3L30R06W1E3_B11 V_{CE} =600 V, I_{Cnom} =30 A
Sixpack Driver	SKHI 61R V_{CE} =900 V, f_{max} =50 kHz
Input Capacitors C_{in}	270 μF, 400 V electrolytic
DC-link Capacitors (Vdc1 - Vdc4)	1000 μF, 160 V electrolytic

SOP technique is used for generating optimal angles for four different operating points (m=.9216, N=4), (m=.5804, N=6), (m=.4706, N=8) and (m=.3059, N=13). Table VI to Table VIII shows the optimal switching angles and division of pulse number N among four 3-level NPC converters for four different operating points based on the analysis in Section IV. Also, optimization criteria is satisfied as can be seen from values of m computed from optimized angles using (9) in Table VI to Table VIII.

For operating point (m=.4706, N=8, f_1=23.53 Hz), pulse number for all three-level NPC inverters is obtained as 2 from Table VIIIa, so the switching frequency of all of them should be equal to $2f_1$. Fig. 9 shows gating signals for one semiconductor device from each of the four three-level NPC inverters and it is clear from the waveforms that each semiconductor device is turned on/off twice in one fundamental period i.e switching frequency is equal to $2f_1$.

Table VI: Optimal switching angles and division of pulse number for (m=.9216, N=4, f_1=46.08 Hz)

	Optimal Angles (Deg)					Pulse Number
Output	0	4.11	11.97	23.13	37.72	N
V_{9L}	0	1	2	3	4	4
V_{5L1}	0	0	0	1	2	2
V_{5L2}	0	1	2	2	2	2
V_{3L11}	0	0	0	0	1	1
V_{3L12}	0	0	0	-1	-1	1
V_{3L21}	0	0	1	1	1	1
V_{3L22}	0	-1	-1	-1	-1	1
$\frac{1}{4}\sum_{i=1}^{4} s(i)\cos(\alpha_i) = .9215 \approx m$						

Table VII: Optimal switching angles and division of pulse number for (m=.5804, N=6, f_1=29.02Hz)

	Optimal Angles (Deg)							Pulse Number
Output	0	28.72	32.33	35.97	46.95	59.29	73.32	N
V_{9L}	0	1	0	1	2	3	4	6
V_{5L1}	0	0	0	0	0	1	2	2
V_{5L2}	0	1	0	1	2	2	2	4
V_{3L11}	0	0	0	0	0	0	1	1
V_{3L12}	0	0	0	0	0	-1	-1	1
V_{3L21}	0	0	0	0	1	1	1	1
V_{3L22}	0	-1	0	-1	-1	-1	-1	3
$\frac{1}{4}\sum_{i=1}^{6} s(i)\cos(\alpha_i) = .5800 \approx m$								

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

Table VIII: Optimal switching angles and division of pulse number *N*

	Optimal Angles (Deg)									Pulse Number
Output	0	4.541	9.570	22.670	28.282	32.838	54.362	66.970	84.844	*N*
V_{9L}	0	1	2	3	4	3	2	1	0	8
V_{5L1}	0	0	0	1	2	1	0	0	0	4
V_{5L2}	0	1	2	2	2	2	2	1	0	4
V_{3L11}	0	0	0	0	1	0	0	0	0	2
V_{3L12}	0	0	0	-1	-1	-1	0	0	0	2
V_{3L21}	0	0	1	1	1	1	1	0	0	2
V_{3L22}	0	-1	-1	-1	-1	-1	-1	-1	0	2
$\frac{1}{4}\sum_{i=1}^{8} s(i)\cos(\alpha_i) = .4709 \approx m$										

(a) (*m*=.4706, *N*=8, f_1=23.53 Hz)

	Optimal Angles (Deg)														Pulse Number
Output	0	3.09	10.0	27.14	31.98	38.36	41.85	44.66	48.05	48.60	49.15	58.625	67.50	85.33	*N*
V_{9L}	0	1	2	1	2	3	2	3	4	3	2	1	0	1	13
V_{5L1}	0	0	0	0	0	1	0	1	2	1	0	0	0	0	6
V_{5L2}	0	1	2	1	2	2	2	2	2	2	2	1	0	1	7
V_{3L11}	0	0	0	0	0	0	0	0	1	0	0	0	0	0	2
V_{3L12}	0	0	0	0	0	-1	0	-1	-1	-1	0	0	0	0	4
V_{3L21}	0	0	1	0	1	1	1	1	1	1	1	0	0	0	4
V_{3L22}	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	-1	3
$\frac{1}{4}\sum_{i=1}^{13} s(i)\cos(\alpha_i) = .3059 \approx m$															

(b) (*m*=.3059, *N*=13, f_1=15.295 Hz)

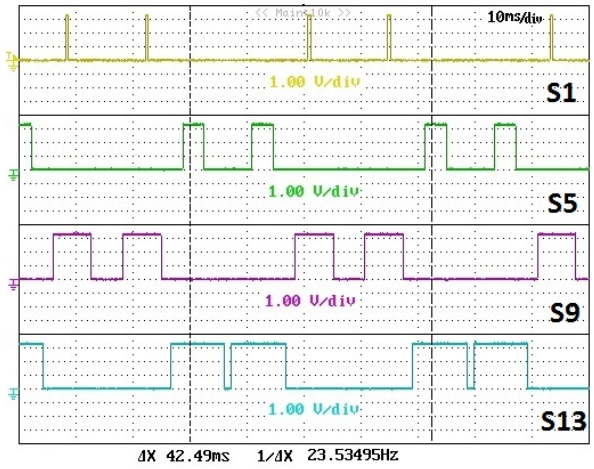
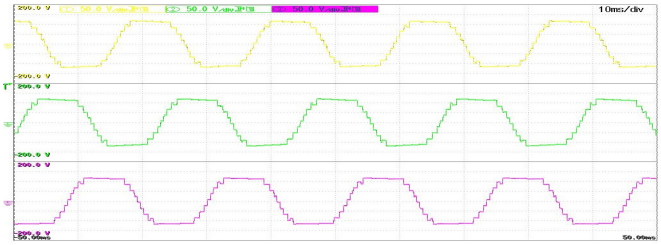


Fig. 9. Gating signals for power semiconductor devices S1, S5, S9 and S13 in phase A

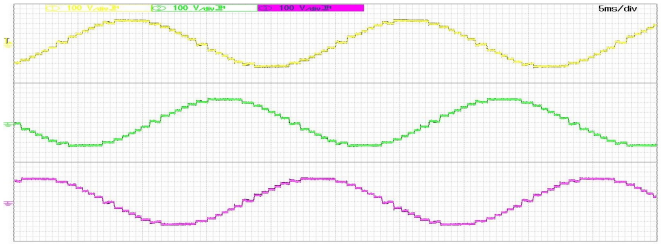
The waveforms of (1) output phase voltages of inverter, (2) line voltages applied to induction motor, (3) stator current, (4) DC-link capacitor voltages of phase B (Vdc1,Vdc2), (5) DC-link capacitor voltages of phase B (Vdc3,Vdc4) (6) NPP error (Vdc1-Vdc2) for top H-Bridge of phase B inverter (7) NPP error (Vdc3-Vdc4) for bottom H-Bridge of phase B inverter pertaining to operating point (*m*=.9216, *N*=4, f_1=46.08 Hz) are shown in Fig. 10. It can be observed that the line voltages and the stator currents of induction motor are nearly sinusoidal even though the switching frequency is only 46.08 Hz. Similar observations about line voltages and stator currents of induction motor corresponding to operating points (*m*=.5804, *N*=6, f_1=29.02Hz), (*m*=.4706, *N*=8, f_1=23.53 Hz) and (*m*=.3059, *N*=13, f_1=15.295 Hz) can be made from Fig. 11 to Fig. 13.

The ripple in DC-link capacitor voltages depends on switching patterns. As explained in Section IV, charging and discharging of DC-link capacitors (Vdc1,Vdc2) and (Vdc3,Vdc4) occurs when the output voltages (V_{5L1}, V_{5L2}) are equal to $\pm V_{dc}$ respectively. From Table VI to Table VIII, it can be observed that minimum and maximum duration for which V_{5L1} or V_{5L2} is equal to V_{dc} corresponds to operating points (*m*=.9216, *N*=4, f_1=46.08 Hz) and (*m*=.3059, *N*=13, f_1=15.295 Hz) respectively. Therefore, minimum peak-to-peak ripple of 2 volts can be seen across DC-link capacitors (Vdc1-Vdc4) corresponding to operating point (*m*=.9216, *N*=4, f_1=46.08 Hz) whereas, maximum peak-to-peak ripple of 6 volts is observed across DC-link capacitors (Vdc3,Vdc4) corresponding to operating point (*m*=.3059, *N*=13, f_1=15.295 Hz). Also, it should be observed from Fig. 10f-10g, Fig. 11f-11g, Fig. 12f-12g, Fig. 13f that average value of NPP error is almost zero. However, there exists a small NPP error of 1.26 volts (4% of DC-link voltage) in bottom H-bridge of phase B inverter as shown in Fig. 13g but it has not affected the harmonic distortion of phase B current waveforms significantly. However, by swapping switching patterns between two NPC legs of phase B the NPP error can be made approximately zero [46]. The efficiency of inverter is observed to be nearly 97% for the all the four different operating points as average device switching frequency is limited to rated fundamental frequency (50 Hz).

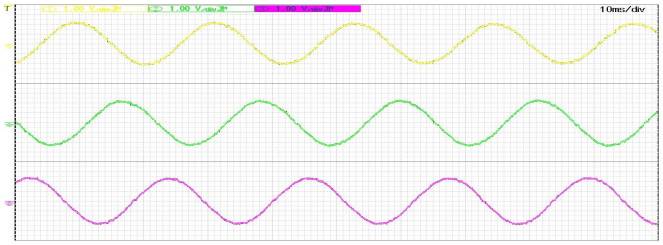
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics



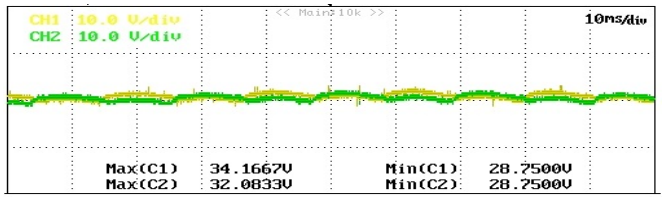
(a) Phase voltages of 9-level inverter



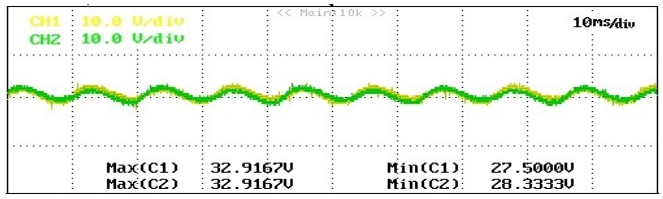
(b) Line voltages of induction motor



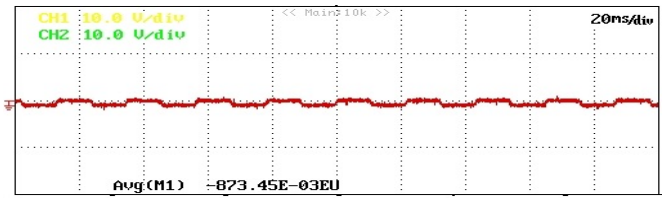
(c) Stator currents of induction motor



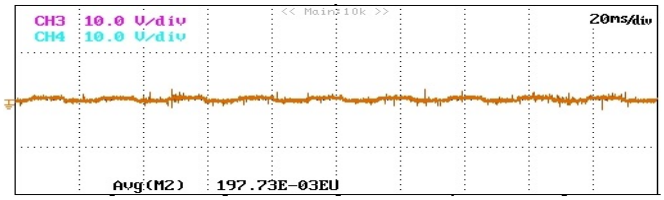
(d) DC-link capacitor voltages (Vdc1,Vdc2) of Phase B inverter



(e) DC-link capacitor voltages (Vdc3,Vdc4) of Phase B inverter

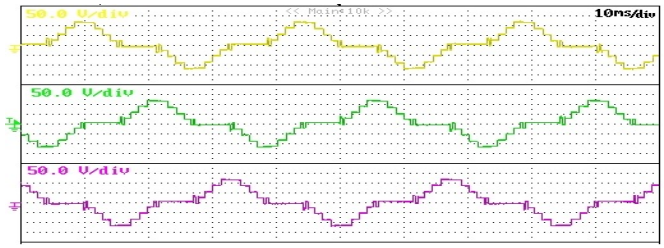


(f) NPP error (Vdc1-Vdc2) for top H-Bridge of Phase B inverter

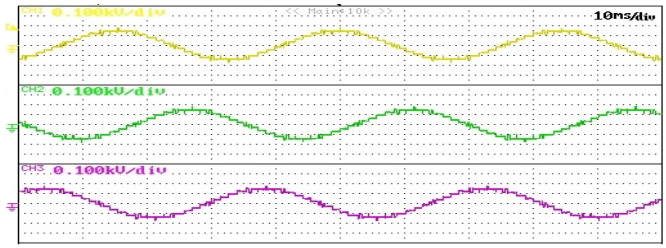


(g) NPP error (Vdc3-Vdc4) for bottom H-Bridge of Phase B inverter

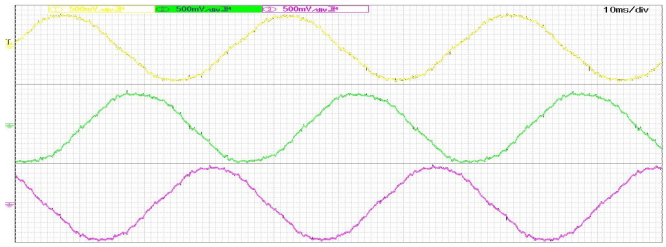
Fig. 10. Experimental results for (m=.9216, N=4)



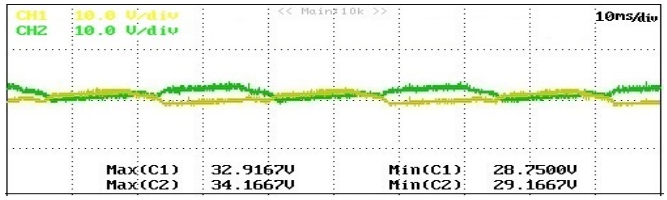
(a) Phase voltages of 9-level inverter



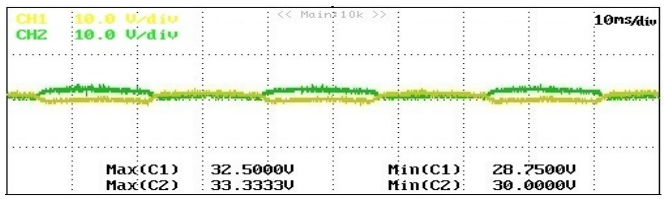
(b) Line voltages of induction motor



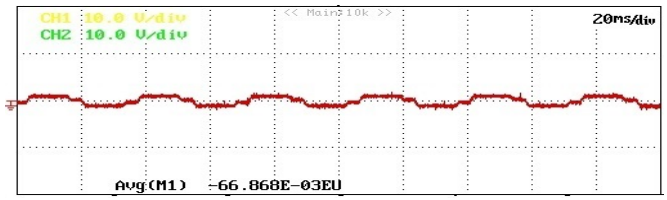
(c) Stator currents of induction motor



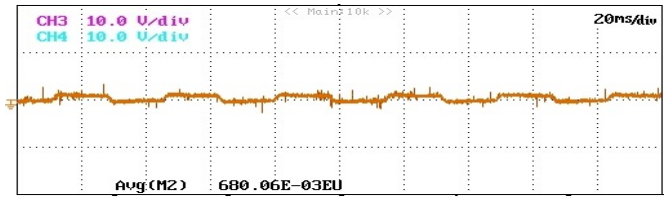
(d) DC-link capacitor voltages (Vdc1,Vdc2) of Phase B inverter



(e) DC-link capacitor voltages (Vdc3,Vdc4) of Phase B inverter



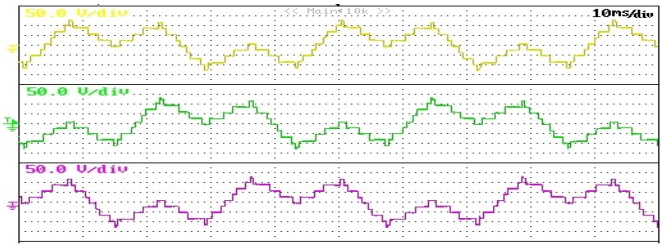
(f) NPP error (Vdc1-Vdc2) for top H-Bridge of Phase B inverter



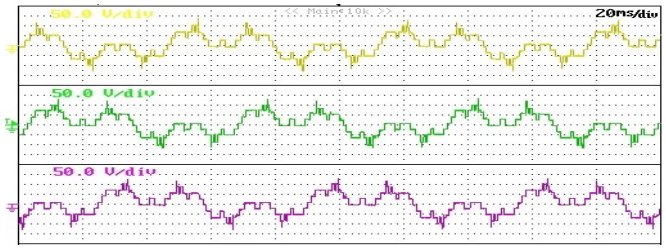
(g) NPP error (Vdc3-Vdc4) for bottom H-Bridge of Phase B inverter

Fig. 11. Experimental results for (m=0.5804, N=6)

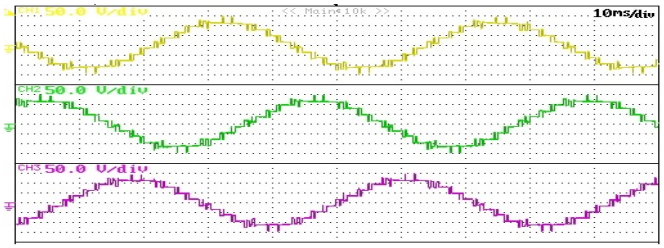
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics



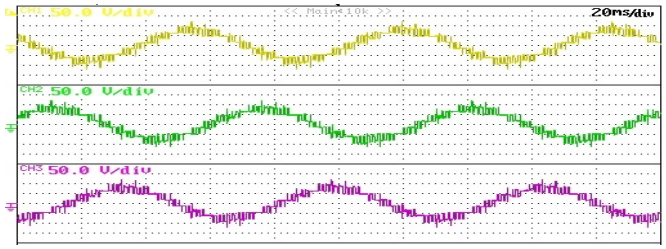
(a) Phase voltages of 9-level inverter



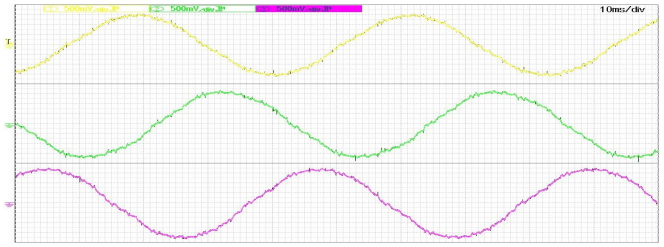
(a) Phase voltages of 9-level inverter



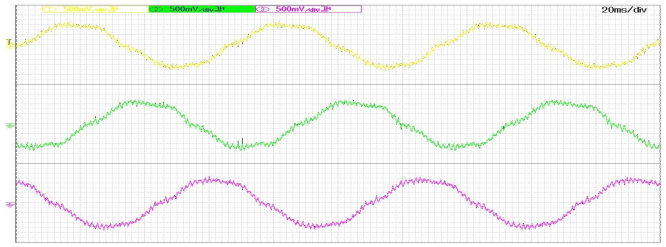
(b) Line voltages of induction motor



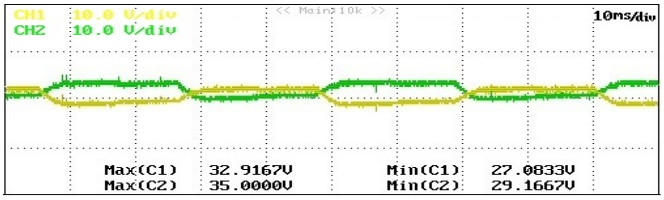
(b) Line voltages of induction motor



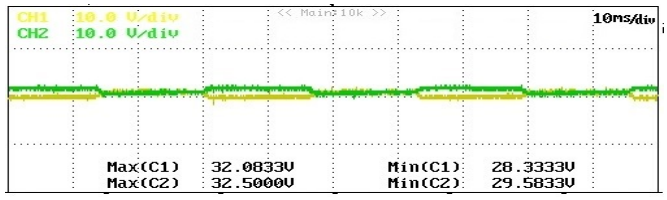
(c) Stator currents of induction motor



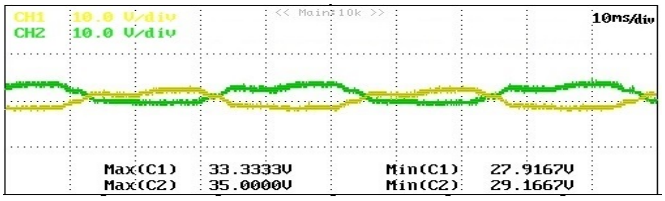
(c) Stator currents of induction motor



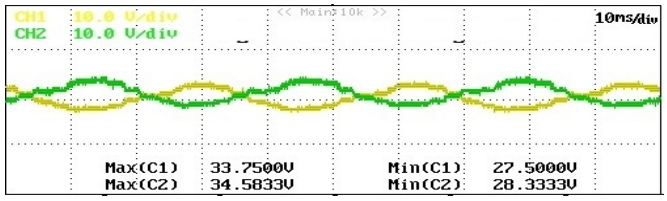
(d) DC-link capacitor voltages (Vdc1,Vdc2) of Phase B inverter



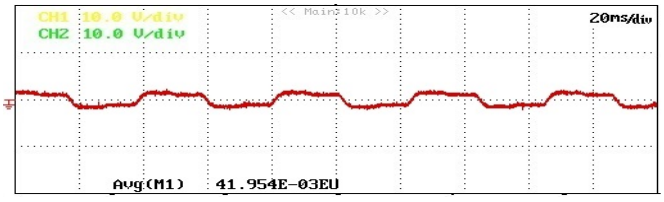
(d) DC-link capacitor voltages (Vdc1,Vdc2) of Phase B inverter



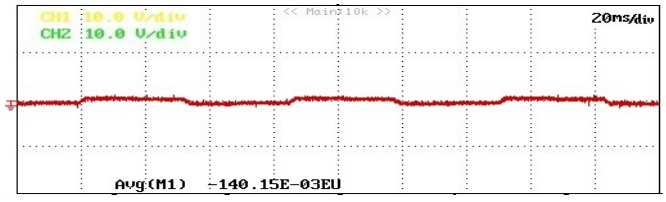
(e) DC-link capacitor voltages (Vdc3,Vdc4) of Phase B inverter



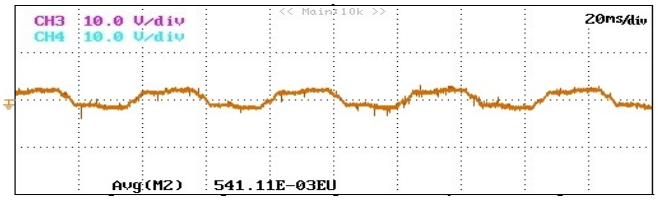
(e) DC-link capacitor voltages (Vdc3,Vdc4) of Phase B inverter



(f) NPP error (Vdc1-Vdc2) for top H-Bridge of Phase B inverter

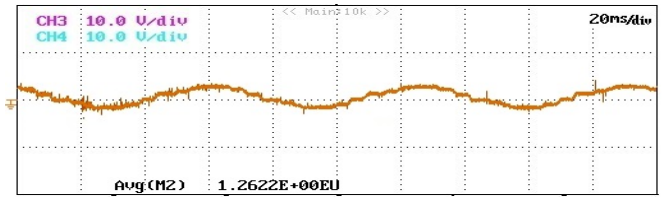


(f) NPP error (Vdc1-Vdc2) for top H-Bridge of Phase B inverter



(g) NPP error (Vdc3-Vdc4) for bottom H-Bridge of Phase B inverter

Fig. 12. Experimental results for (m=.4706, N=8)

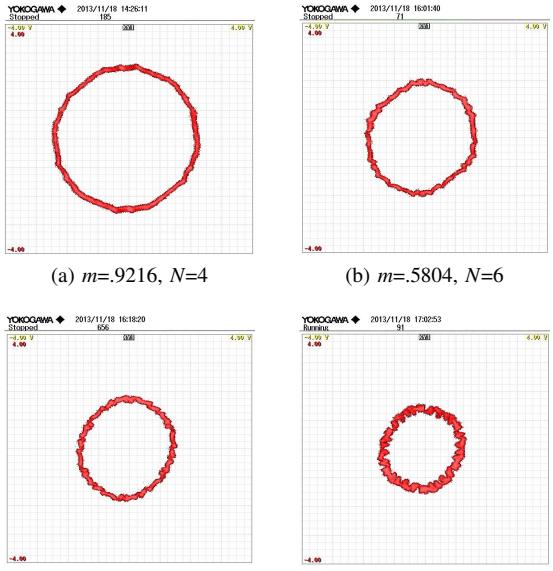


(g) NPP error (Vdc3-Vdc4) for bottom H-Bridge of Phase B inverter

Fig. 13. Experimental results for (m=.3059, N=13)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

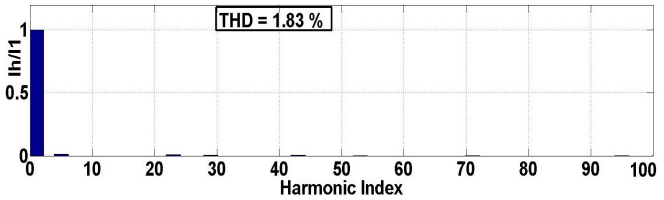
The Space vector trajectory of stator currents for four operating points is shown in Fig. 14 and almost circular trajectories indicate lesser harmonic distortion. In addition, data acquisition system is used to record the stator currents in to a PC and then data is further processed to calculate the harmonic components as well as THD. The values of THD between 2-5% for all operating points as shown in Fig. 15 indicates that by using SOP technique it is possible to limit average device switching frequency to rated fundamental frequency (50 Hz) while keeping THD below standard limits.



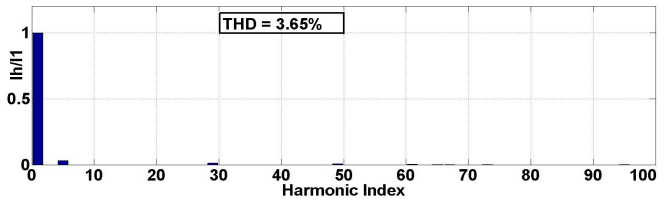
(a) m=.9216, N=4 (b) m=.5804, N=6

(c) m=.4706, N=8 (d) m=.3059, N=13

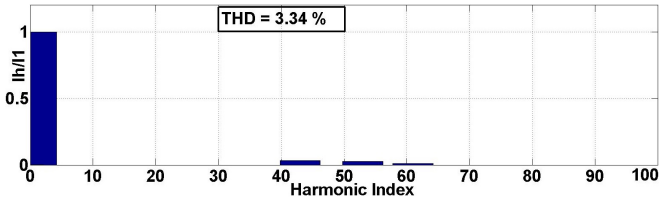
Fig. 14. Space vector trajectory of stator currents



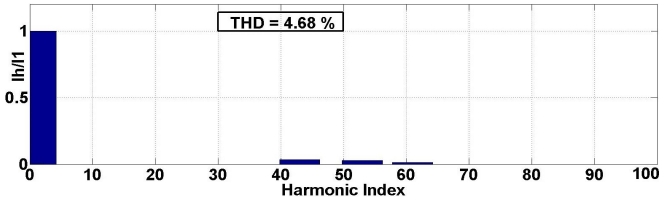
(a) m=.9216, N=4



(b) m=.5804, N=6



(c) m=.4706, N=8



(d) m=.3059, N=13

Fig. 15. FFT plots for phase A stator current

VI. Conclusion

Cascade NPC H-bridge topology is selected for implementing nine-level inverter due to limitations of NPC and FC topologies. Low switching frequency operation of multilevel inverters is essential to reduce the switching losses in medium voltage high power applications. Proposed SOP technique permits multilevel inverter to operate at an average device switching frequency limited to rated fundamental frequency without compromising on harmonic distortion. Optimal nine-level waveforms are produced using SOP technique and then switching instants for each semiconductor device is determined based on the criteria to reduce device switching frequency as well as to ensure minimal unbalance in the DC-link capacitor voltages. Experimental results for four different operating points demonstrate effectiveness of the proposed modulation in limiting average device switching frequency to rated fundamental frequency without compromising on THD as well as resulting in low ripple at DC-link voltages. Compared to other low switching frequency control algorithms for nine-level inverter like model predictive control (f_s = 425 to 500 Hz) [16] and adaptive duty-cycle modulation algorithm (f_s= 285 to 785 Hz) [17], the switching frequency of operation has been reduced more than five times without compromising on THD of current waveforms.

References

[1] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters -state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581 –2596, aug. 2010.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553 –2580, aug. 2010.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, july 2010.

[4] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219 –2230, july 2010.

[5] J. Rodriguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, and M. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786 –1817, nov. 2009.

[6] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28 –39, june 2008.

[7] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930 –2945, dec. 2007.

[8] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 36–44, 1999.

[9] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power

converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509 –517, may/jun 1996.

[10] S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected h-bridge multilevel converters," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1032 –1040, july-aug. 2007.

[11] W. Hill and C. Harbourt, "Performance of medium voltage multi-level inverters," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, vol. 2, 1999, pp. 1186–1192 vol.2.

[12] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuits," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2111–2124, 2013.

[13] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3482 –3494, aug. 2012.

[14] Z. Cheng and B. Wu, "A novel switching sequence design for five-level npc/h-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2138 –2145, nov. 2007.

[15] Z. Du, L. Tolbert, B. Ozpineci, and J. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 25–33, 2009.

[16] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded h-bridge inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2691–2699, 2010.

[17] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching-frequency-modulation algorithm for high-power multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2894 –2901, oct. 2007.

[18] H. S. Patel and R. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part i–harmonic elimination," *IEEE Transactions on Industry Applications*, vol. IA-9, no. 3, pp. 310–317, 1973.

[19] ——, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part ii — voltage control techniques," *IEEE Transactions on Industry Applications*, vol. IA-10, no. 5, pp. 666–673, 1974.

[20] I. Pitel, S. N. Talukdar, and P. Wood, "Characterization of programmed-waveform pulsewidth modulation," *IEEE Transactions on Industry Applications*, vol. IA-16, no. 5, pp. 707–715, 1980.

[21] P. Enjeti, P. Ziogas, and J. Lindsay, "Programmed pwm techniques to eliminate harmonics: a critical evaluation," *IEEE Transactions on Industry Applications*, vol. 26, no. 2, pp. 302–316, 1990.

[22] A. Maheshwari and K. D. T. Ngo, "Synthesis of six-step pulsewidth-modulated waveforms with selective harmonic elimination," *IEEE Transactions on Power Electronics*, vol. 8, no. 4, pp. 554–561, 1993.

[23] F. Swift and A. Kamberis, "A new walsh domain technique of harmonic elimination and voltage control in pulse-width modulated inverters," *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 170–185, 1993.

[24] T.-J. Liang, R. O'Connell, and R. Hoft, "Inverter harmonic reduction using walsh function harmonic elimination method," *IEEE Transactions on Power Electronics*, vol. 12, no. 6, pp. 971–982, 1997.

[25] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 491–499, 2004.

[26] J. Wells, B. Nee, P. Chapman, and P. Krein, "Selective harmonic control: a general problem formulation and selected solutions," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1337–1345, 2005.

[27] V. Blasko, "A novel method for selective harmonic elimination in power electronic equipment," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 223–228, 2007.

[28] V. Agelidis, A. Balouktsis, I. Balouktsis, and C. Cossar, "Multiple sets of solutions for harmonic elimination pwm bipolar waveforms: analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 415–421, 2006.

[29] J. Wells, X. Geng, P. Chapman, P. Krein, and B. Nee, "Modulation-based harmonic elimination," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 336–340, 2007.

[30] G. Poddar and M. Sahu, "Natural harmonic elimination of square-wave inverter for medium-voltage application," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1182–1188, 2009.

[31] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "A unified approach to solving the harmonic elimination equations in multilevel converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 478–490, 2004.

[32] A. Kavousi, B. Vahidi, R. Salehi, M. Bakhshizadeh, N. Farokhnia, and S. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1689–1696, 2012.

[33] A. Rathore, J. Holtz, and T. Boller, "Generalized optimal pulsewidth modulation of multilevel inverters for low switching frequency control of medium voltage high power industrial ac drives," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4215–4224, 2013.

[34] ——, "Synchronous optimal pulsewidth modulation for low-switching-frequency control of medium-voltage multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2374 –2381, july 2010.

[35] T. Boller, J. Holtz, and A. Rathore, "Optimal pulsewidth modulation of a dual three-level inverter system operated from a single dc link," *IEEE Transactions on Industry Applications*, vol. 48, no. 5, pp. 1610–1615, 2012.

[36] J. Holtz and N. Oikonomou, "Optimal control of a dual three-level inverter system for medium-voltage drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 3, pp. 1034 –1041, may-june 2010.

[37] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulsewidth modulation," *IEEE Transactions on Industry Applications*, vol. 31, no. 5, pp. 1110 –1120, sep/oct 1995.

[38] ——, "The trajectory tracking approach-a new method for minimum distortion pwm in dynamic high-power drives," *IEEE Transactions on Industry Applications*, vol. 30, no. 4, pp. 1048 –1057, jul/aug 1994.

[39] J. Holtz and N. Oikonomou, "Estimation of the fundamental current in low-switching-frequency high dynamic medium-voltage drives," *IEEE Transactions on Industry Applications*, vol. 44, no. 5, pp. 1597 –1605, sept.-oct. 2008.

[40] ——, "Fast dynamic control of medium voltage drives operating at very low switching frequency - an overview," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1005 –1013, march 2008.

[41] N. Oikonomou and J. Holtz, "Closed-loop control of medium-voltage drives operated with synchronous optimal pulsewidth modulation," *IEEE Transactions on Industry Applications*, vol. 44, no. 1, pp. 115 –123, jan.-feb. 2008.

[42] J. Holtz and N. Oikonomou, "Synchronous optimal pulsewidth modulation and stator flux trajectory control for medium-voltage drives," *IEEE Transactions on Industry Applications*, vol. 43, no. 2, pp. 600 –608, march-april 2007.

[43] J. Holtz and B. Beyer, "Optimal synchronous pulsewidth modulation with a trajectory-tracking scheme for high-dynamic performance," *IEEE Transactions on Industry Applications*, vol. 29, no. 6, pp. 1098–1105, 1993.

[44] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE*, vol. 82, no. 8, pp. 1194 –1214, aug 1994.

[45] G. S. Buja, "Optimum output waveforms in pwm inverters," *IEEE Transactions on Industry Applications*, vol. IA-16, no. 6, pp. 830 –836, nov. 1980.

[46] T. Boller, J. Holtz, and A. Rathore, "Neutral point potential balancing using synchronous optimal pulsewidth modulation of multilevel in medium voltage high power ac drives," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2013.

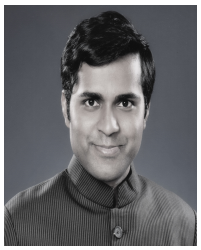
[47] J. Holtz and N. Oikonomou, "Neutral point potential balancing algorithm at low modulation index for three-level inverter medium-voltage drives," *IEEE Transactions on Industry Applications*, vol. 43, no. 3, pp. 761 –768, may-june 2007.

[48] H. Du Toit Mouton, "Natural balancing of three-level neutral-point-clamped pwm inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1017–1025, 2002.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2014.2298239, IEEE Transactions on Power Electronics

Amarendra Edpuganti (S'13) received the B.Tech. degree in Electrical and Electronics Engineering from National Institute of Technology, Warangal, India in 2007 and the M.Tech degree in Electrical Engineering from Indian Institute of Technology, Kanpur, India in 2012. He worked as software engineer with Adobe Systems Inc., Bangalore, India from Aug 2007 to Dec 2009. He is currently working towards his Ph.D. degree in the area of Power Electronics at Electrical and Computer Engineering, National University of Singapore.

His research interests include multilevel power converters, pulsewidth modulation techniques, and wind power integration.



Akshay Kumar Rathore (M'05-SM'12) received his Masters degree in Electrical Machines and Drives from Indian Institute of Technology (BHU), Varanasi, India in 2003. He was awarded Gold Medal for securing highest academic standing among all the electrical engineering specializations. He obtained PhD in Power Electronics from University of Victoria, Victoria, BC, Canada in 2008. He was a recipient of PhD fellowship and Thouvenelle Graduate Scholarship during his PhD study. He has two subsequent postdoctoral research appointments with University of Wuppertal, Germany from Sept. 2008-Aug. 2009 and University of Illinois at Chicago, USA from Sept. 2009 - Sept. 2010.

Since Nov 2010 he is an Assistant Professor in Department of Electrical and Computer Engineering, National University of Singapore. He is responsible for teaching and research in the area of power electronics systems. He has developed new courses on advanced power electronics, advanced control of electrical drives, and smart grid.

His research interests mainly include analysis, design, and development of current-fed converter technologies for renewable energy and electric transportation applications, soft-switching schemes and PWM modulation techniques for high frequency power converters, optimal low switching frequency control of medium voltage multilevel inverters. He has been actively researching on novel and innovative current-fed topologies and modulation techniques and has published heavily in this area. He has published 70 research papers in international journals and conferences.

He is an Associate Editor of IEEE Transactions on Industry Applications, IEEE Journal of Emerging Selected Topics in Power Electronics, and International Journal of Power Electronics. He is an editor of Electric Power Components and Systems. He has been a guest Associate Editor for special issue on transportation electrification and vehicle systems in IEEE Transaction on Power Electronics, appeared on December 2013 issue. He is a guest Associate Editor for special issue on transportation electrification in IEEE Journal on Emerging Selected Topics in Power Electronics.

He delivered tutorials on current-fed converters for renewable energy and clean transportation at IEEE Industrial Symposium on Industrial Electronics (ISIE) 2012 held in Hangzhou, China, IEEE Power Electronics, Drives, and Energy Systems (PEDES) 2012 Conference held in Bangalore, India, and IEEE International Conference on Sustainable Energy Technologies (ICSET) 2012 held in Kathmandu, Nepal. He has served as a Technical Track Chair for IEEE Industrial Electronics Conference (IECON) 2012 held in Montreal, Canada, IECON 2013 to be held in Vienna, Austria, IEEE Power Electronics and Drive Systems (PEDS) 2013 held in Kitakyushu, Japan, and IEEE ISIE 2014 to be held in Istanbul, Turkey. He was Tutorial Chair for PEDS 2011 held in Singapore and ICSET 2012 held in Kathmandu, Nepal.

Dr. Rathore is a winner and recipient of 2013 IEEE IAS Andrew W Smith Outstanding Young Member Award. He is first working in Asia to receive this award. Dr. Rathore has been listed in Marquis Whos Who in Science and Engineering in 2006, Whos Who in the World, and Whos Who in America in 2008