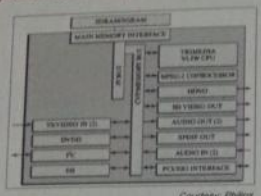
امروزه چیپ ها یا chips در قسمتهای مختلف هستند
SSE - PC - DVD

A System-on-a-Chip: Example



Courtesy: Philips

Digital Integrated Circuits
A Design Perspective

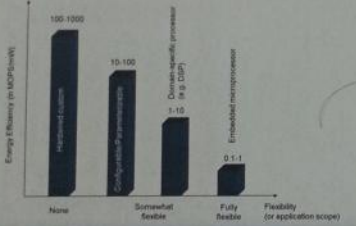
Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Design Methodologies

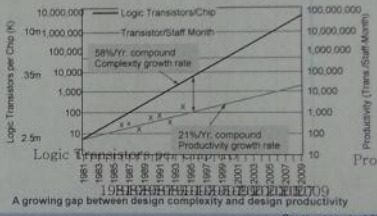
December 10, 2002

مقایسه طراحی پیاده سازی
Impact of implementation
توقعی هم چیزا در تراشه متراکم می کنیم که صرف انرژی پایین
بیاید و سرعت بالا می رود و صرف توان هم کم می شود

Impact of Implementation Choices



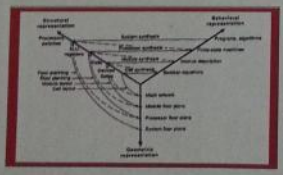
The Design Productivity Challenge



سرعت رشد تراشه ها روز به روز زیادتر می شود.

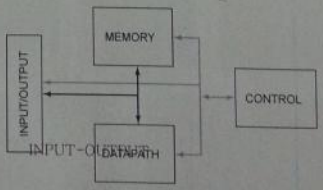
روشهای طراحی:
اگر بخواهیم یک برنامه را طراحی کنیم باروشهای سنتی مدت زیادی
طول می کشد اما نرم افزارهای وجود دارند که این کار را
می کنند و روشهایی است که این کار را ساده می کنند

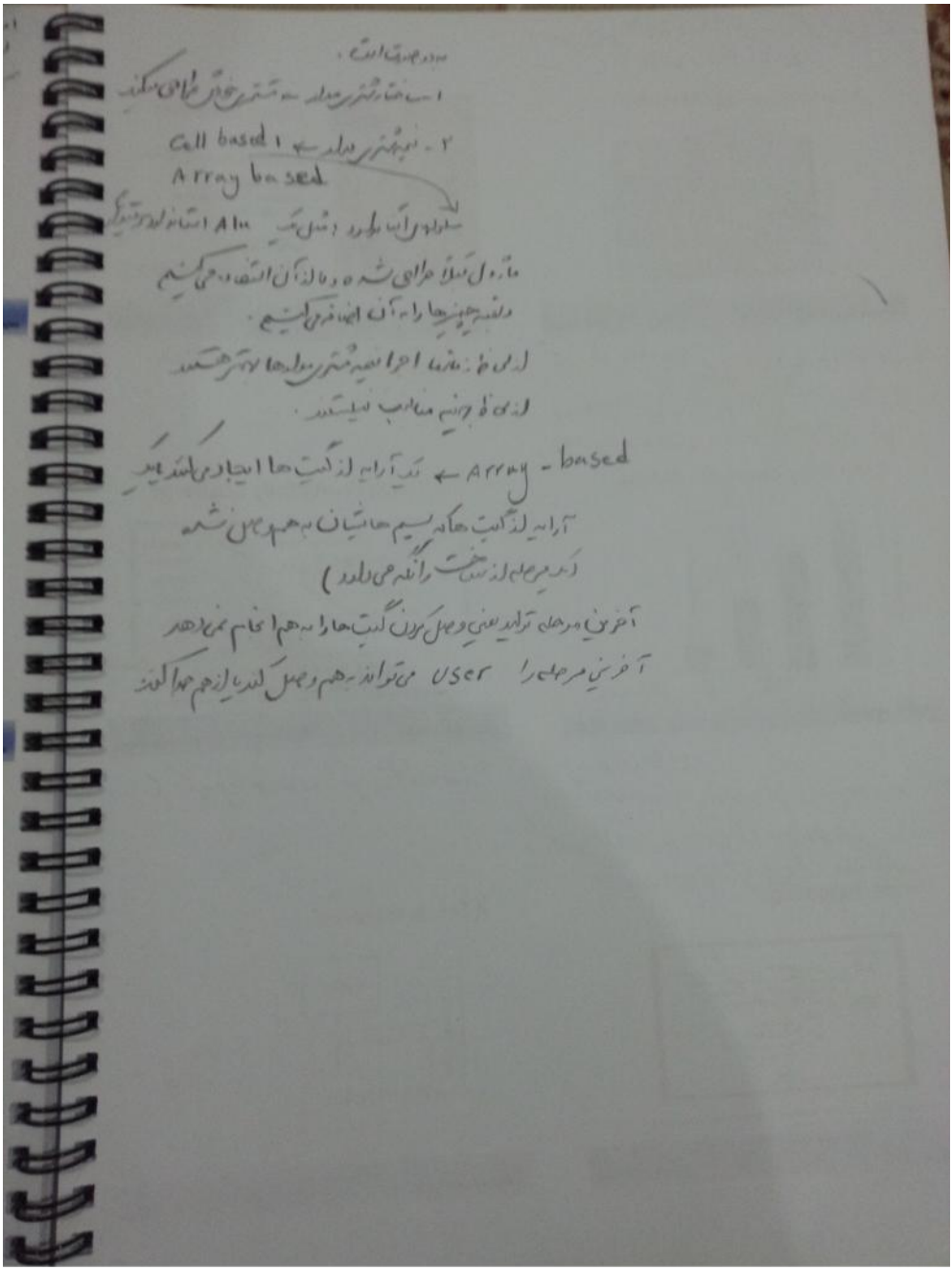
Design Methodology

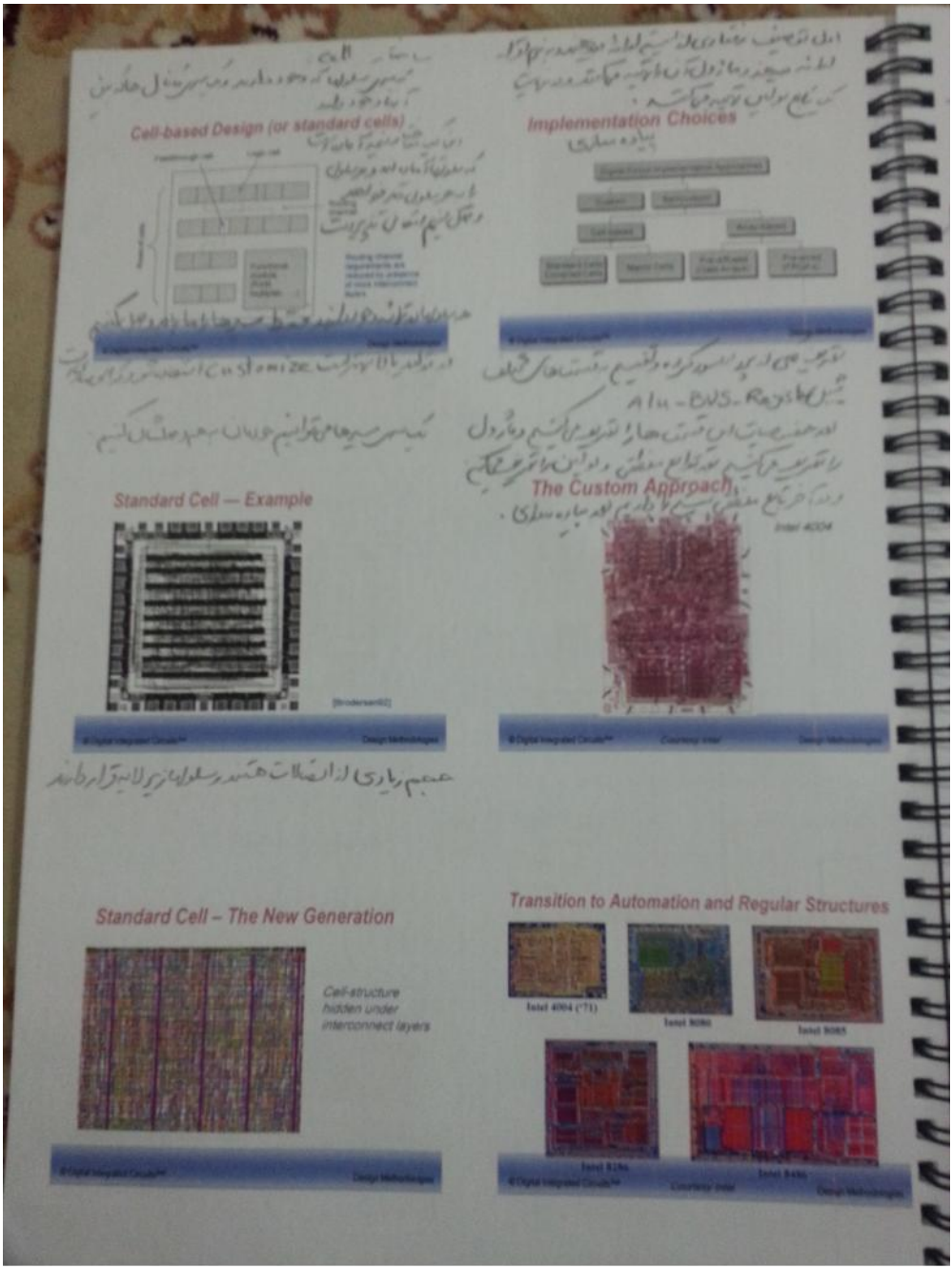


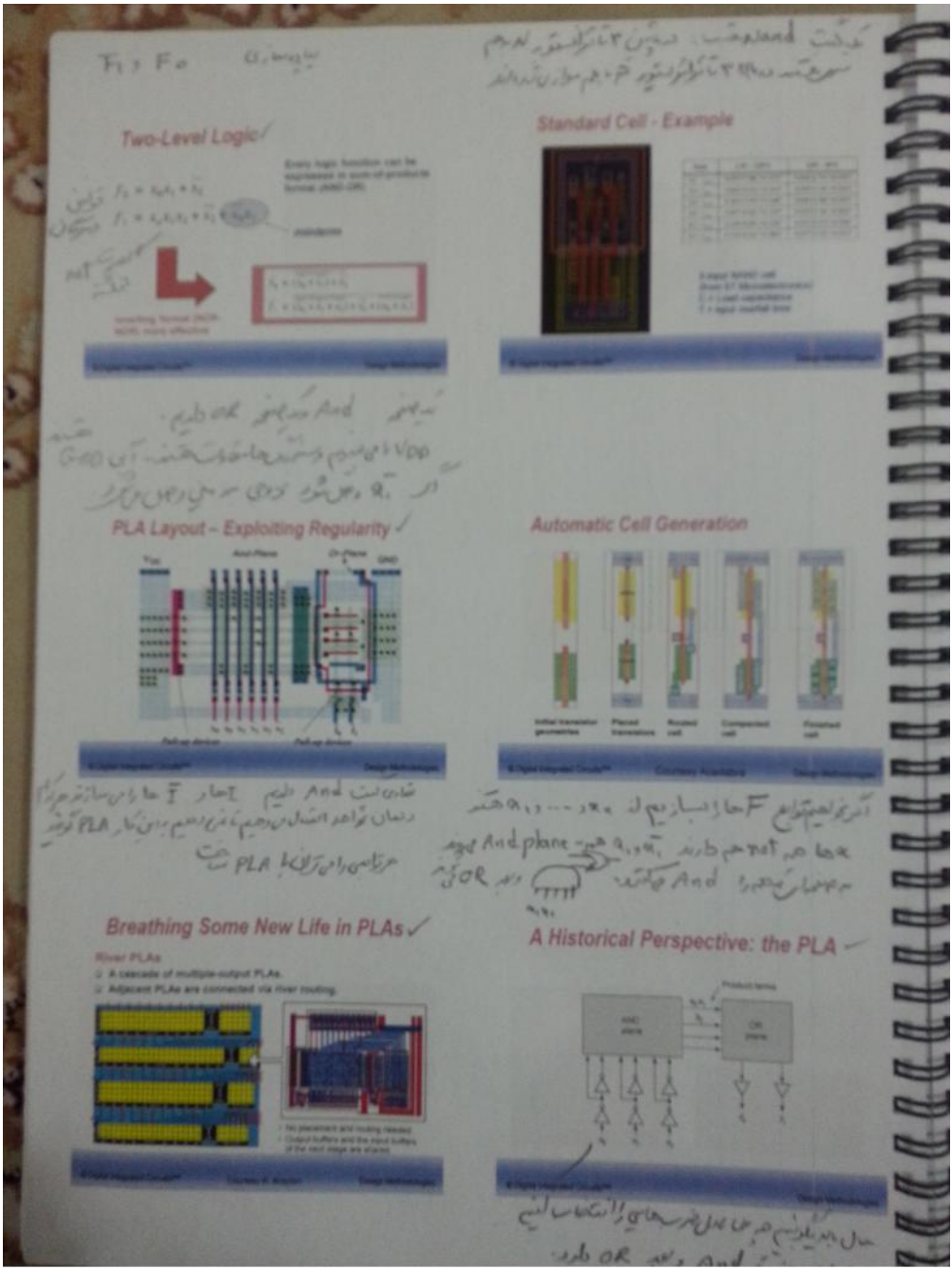
- Design process traverses iteratively between three abstractions: behavior, structure, and geometry
- More and more automation for each of these steps

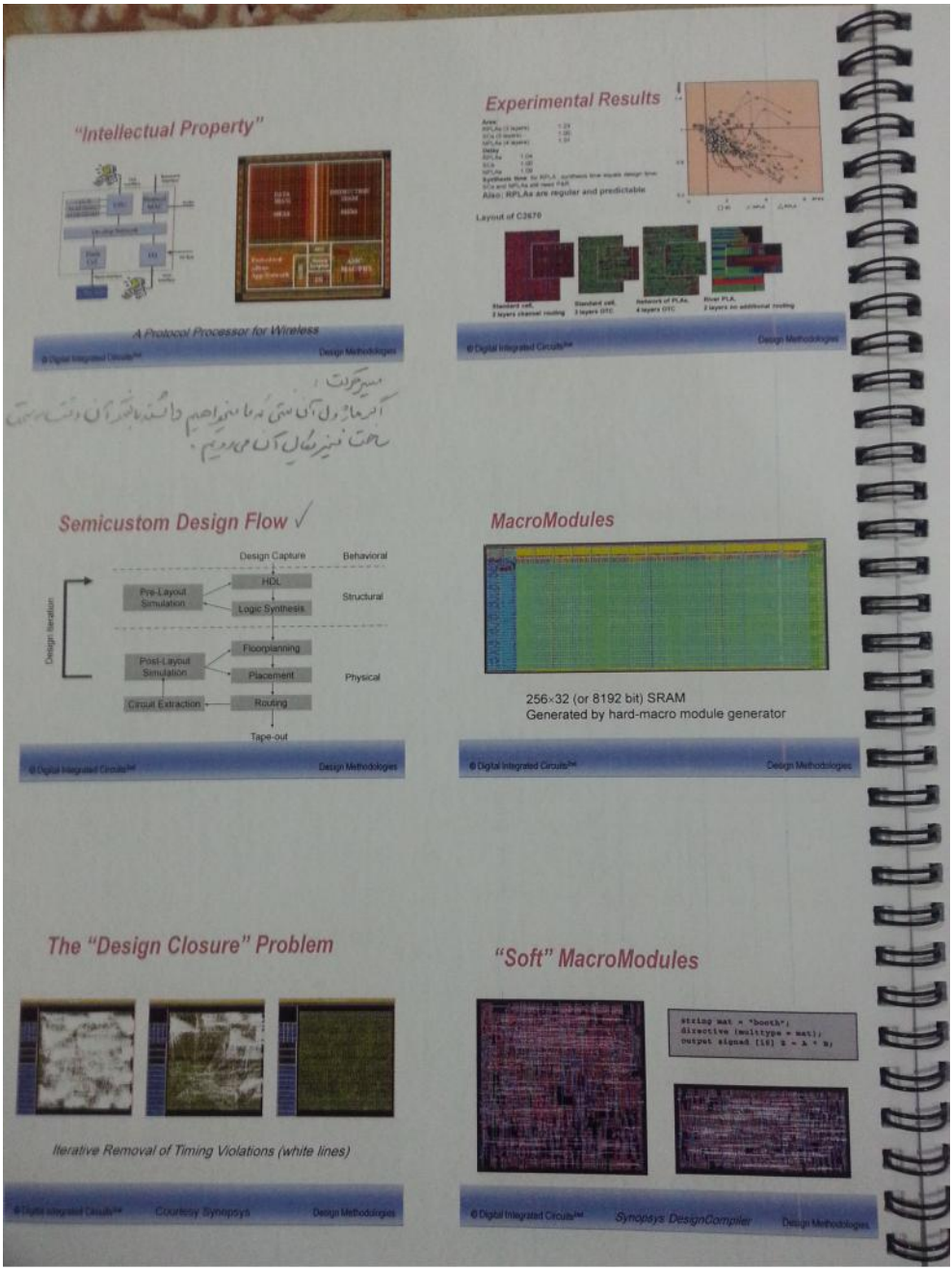
A Simple Processor

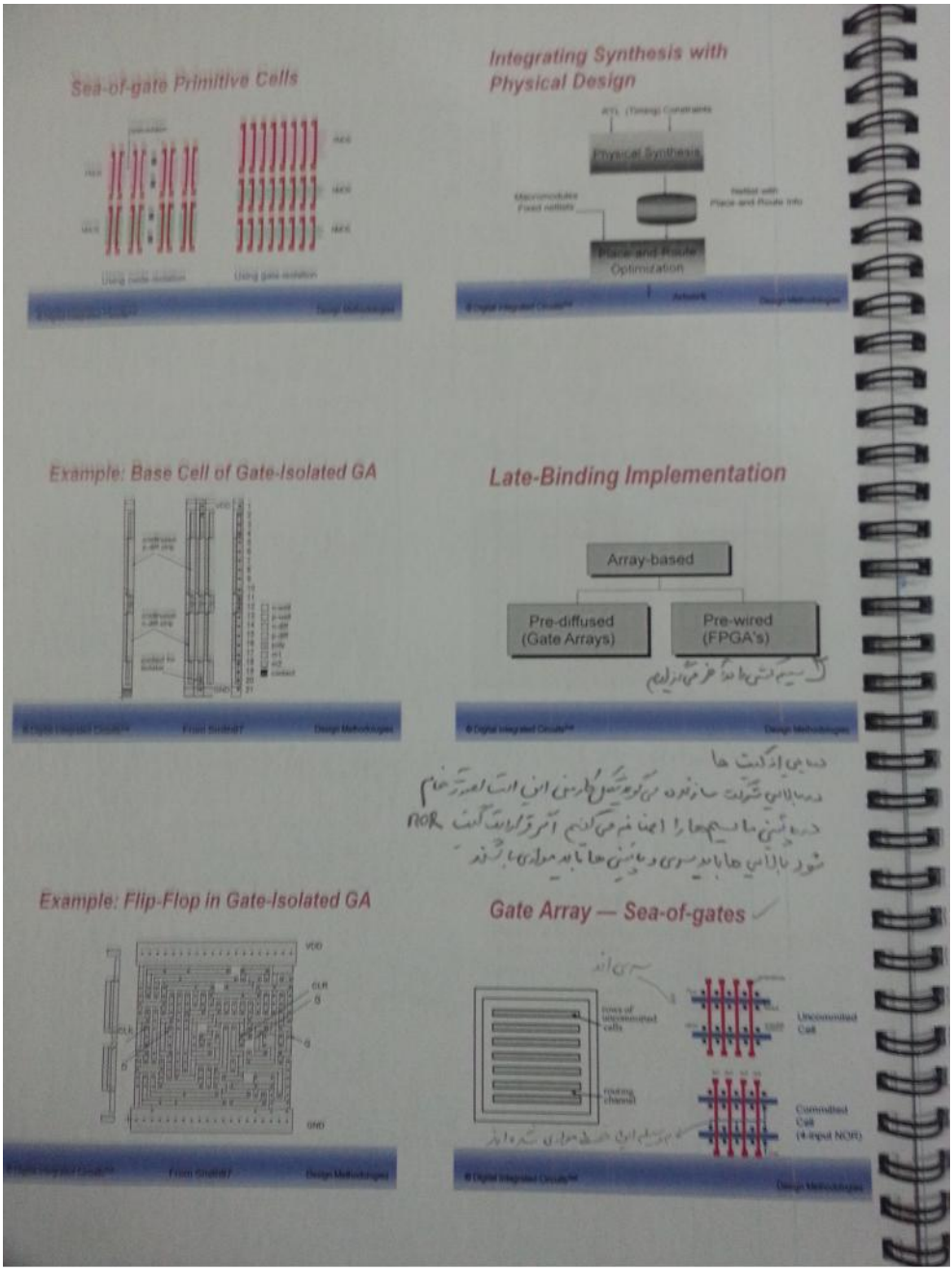





Cell-based Design (or standard cells)
Implementation Choices
Standard Cell — Example
The Custom Approach
Standard Cell – The New Generation
Cell-structure hidden under interconnect layers
Transition to Automation and Regular Structures

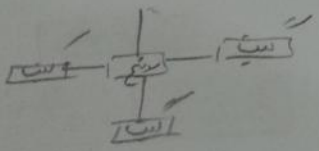

Two-Level Logic
Standard Cell - Example
PLA Layout – Exploiting Regularity
Automatic Cell Generation
Breathing Some New Life in PLAs
A Historical Perspective: the PLA


"Intellectual Property"
A Protocol Processor for Wireless
Experimental Results
Also, RPLAs are regular and predictable
Layout of C2670
Semicustom Design Flow
Design Capture
Behavioral
HDL
Pre-Layout Simulation
Logic Synthesis
Structural
Design Iteration
Floorplanning
Post-Layout Simulation
Placement
Physical
Circuit Extraction
Routing
Tape-out
MacroModules
256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator
The "Design Closure" Problem
Iterative Removal of Timing Violations (white lines)
Courtesy Synopsys
"Soft" MacroModules
Synopsys DesignCompiler
Design Methodologies


Sea-of-gate Primitive Cells
Integrating Synthesis with Physical Design
Physical Synthesis
Place and Route Optimization
Example: Base Cell of Gate-Isolated GA
Late-Binding Implementation
Array-based
Pre-diffused (Gate Arrays)
Pre-wired (FPGA's)
Example: Flip-Flop in Gate-Isolated GA
Gate Array — Sea-of-gates
Uncommitted Cell
Committed Cell (4-input NOR)

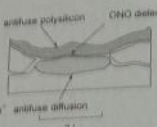
PLA : در خروجی OR ها شصت چهار تا OR داریم.

بین میرها متفاوت است:
سلولهای حافظه را با سه تریج ها به هم وصل می کنیم
حجم تراشه زیاد می شود ولی خوبی دارای است که در
اختیار دارد و هر طراحی که بخواهیم تریج ها را وصل
می کنیم یعنی با سه تریج ها گیت ها را به هم وصل می کنیم



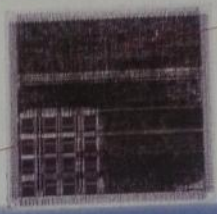
هر برنامه را نیاز داریم استفاده می کنیم و بعضی را می سازیم
در ساختارهای توصیفی گیت And , OR و
فیوز داریم.

Fuse-Based FPGA



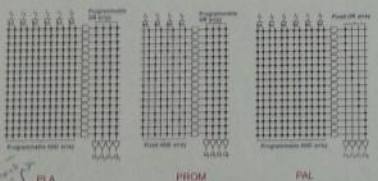
Open by default, closed by applying current pulse

Sea-of-gates

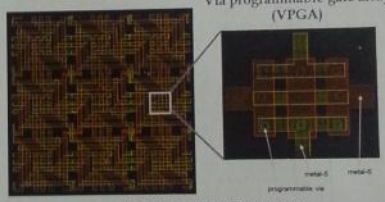


Courtesy LSI Logic

Array-Based Programmable Logic

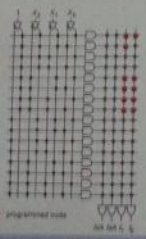


The return of gate arrays?



Exploits regularity of interconnect

Programming a PROM



$$f_0 = x_0x_1 + \overline{x}_2$$

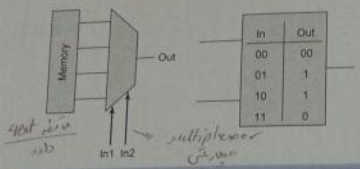
$$f_1 = x_0x_1x_2 + \overline{x}_2 + \overline{x}_0x_1$$

Prewired Arrays

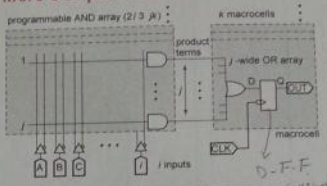
Classification of prewired arrays (or field-programmable devices):

- Based on Programming Technique
  - Fuse-based (program-once)
  - Non-volatile EPROM based
  - RAM based
- Programmable Logic Style
  - Array-Based
  - Look-up Table
- Programmable Interconnect Style
  - Channel-routing
  - Mesh networks

Look-up Table Based Logic Cell

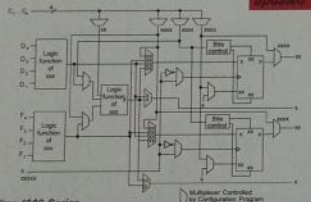


More Complex PAL



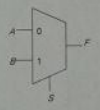
LUT-Based Logic Cell

Figure must be updated



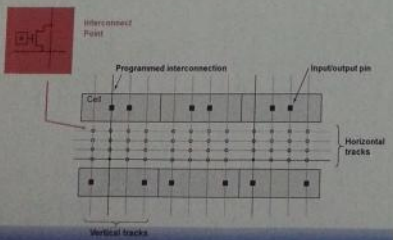
Xilinx 4000 Series

2-input mux as programmable logic block



Configuration			
A	B	S	F=
0	0	0	0
0	X	1	X
0	Y	1	Y
0	Y	X	XY
X	0	Y	XY
Y	0	X	XY
Y	1	X	X + Y
1	0	X	X
1	0	Y	Y
1	1	1	1

Array-Based Programmable Wiring



Logic Cell of Actel Fuse-Based FPGA