

Novel Reversible Fault Tolerant Error Coding and Detection Circuits

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Abstract: Reversible logic is an emerging area of research, having applications in nanotechnology, low power CMOS design, quantum computing and DNA computing. In this paper two different parity preserving reversible error coding and detection circuits are studied. First we propose two new reversible Hamming code generator circuits. One of them is parity preserve. We also propose a new parity preserving reversible Hamming code error detector circuit. The proposed parity preserving reversible Hamming code generator and error detector circuits provide single error correction-double error detection (SEC-DED). The designs are better than the existing counterparts in term of quantum cost, number of constant inputs and number of garbage outputs. Then we propose parity preserving reversible cyclic code encoder/decoder circuits for the first time. A parity preserving reversible D flip-flop is also proposed. Equivalent quantum representation of two parity preserving 4*4 reversible gates, IG and PPHCG, are also proposed. We show for the first time that IG has a quantum cost of only 7 and PPHCG has a quantum cost of only 6.

Keywords: Quantum computation, reversible logic design, fault tolerance, Hamming code, cyclic code, low power design, parity preserving reversible circuits, Nanotechnology.

1- Introduction

Traditional irreversible circuits have power dissipations regardless of their realization techniques [1]. This is due to the information loss. It is proved that for every bit of information that is lost during a computation, $KT \ln 2$ Joules of energy dissipates, where $K=1.3806505 \cdot 10^{-23} \text{m}^2 \text{kg}^{-2} \text{K}^{-1}$ (Joules/Kelvin) is the Boltzmann's constant and T is the absolute temperature at which operation is performed [2]. In fact, irreversibility means heat generation. One of the advantages of reversible logic design is that it has theoretically zero internal power dissipation because it does not lose information. On the other hand, reversible logic design is an interesting and important area of study because it is necessary in quantum technologies. Quantum gates are introduced based on quantum computing theory. Quantum circuits are reversible because a closed quantum mechanical system is inherently reversible [3-4]. Reversible logic circuit implementations are also found in nanotechnology, low power CMOS design, optical information processing, quantum computing, thermodynamics, adiabatic CMOS and DNA computing. A circuit is reversible if and only if the input vector can be uniquely recovered from the output vector. That is, there is a one-to-one mapping between its input and output vectors. Thus, a reversible logic circuit has equal number of inputs and outputs. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [4-9].

The 1×1 and 2×2 quantum gates are realized in some quantum techniques [10]. However, we can't directly realize the bigger quantum gates (such as 3×3 gates) in quantum technology. Thus, we use the 1×1 and 2×2 gates to implement the bigger ones. The quantum cost (QC) of a reversible or quantum circuit is defined as the number of 1×1 or 2×2 gates used to implement the circuit [4].

Conventional gates (such as AND, NAND, OR, etc.), are not reversible. Some restrictions are assumed to reversible circuits. Feedback and fan-out are forbidden in reversible logic. Consequently, synthesis of a reversible logic circuit is significantly more complicated than the conventional circuits. Some reversible logic circuit synthesis methods are proposed in the past decades [3, 11].

Some factors such as the amount of garbage outputs, the number of constant inputs, size of the circuit and quantum cost (QC) are very important criterions in reversible logic design and we should try to minimize them [4, 9, 12-14]. It is also more difficult to make a fault-tolerant reversible circuit than a conventional logic circuit [15-16].

If a system is made up of fault tolerant components, then it will be able to continue operating properly when the failure occurs in some of its components. The detection and correction of faults in such fault tolerant systems are easier. We can achieve fault tolerance in many systems by using parity bits. Thus,

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parity preserving reversible circuit design will be very important for development of fault tolerant reversible systems in nanotechnology which is an emerging technology [17].

There exists several error correcting codes (ECC). One of the most commonly used codes to construct single-error-correcting and double-error-detecting (SEC-DEC) code is the Hamming Code [18].

In this paper we propose low power circuits implemented using reversible logic that provides single-error-correction and double-error-detection (SEC-DEC). Two new reversible Hamming code generator circuits are proposed. One of them is parity preserving reversible circuit. We also propose a new parity preserving reversible Hamming code error detector circuit. These designs are better than the existing designs in the sense of above mentioned complexity factors.

We also propose parity preserving reversible (7, 4) cyclic code encoder/decoder circuits. A parity preserving reversible D flip-flop, and equivalent quantum representation of two parity preserving 4*4 reversible gates, IG and PPHCG, are also proposed. We show for the first time that IG has a quantum cost of only 7 and PPHCG has a quantum cost of only 6. Parity preserving reversible PPHCG gate is used in some of the previous designs which are compared with our new designs. Therefore it is important to have PPHCG quantum realization for a fair comparison of the existing designs with our new designs.

The organization of the paper is as follows: Section 2 covers the basic concepts including reversible logic gates and circuits, quantum gates and circuits, and parity preserving reversible gates and circuits.

Our proposed quantum realization of parity preserving reversible IG gate and PPHCG gate are presented in section 3 and 4 respectively. Our proposed reversible hamming code generator, parity preserving reversible hamming code generator, and parity preserving reversible hamming code error detector are also presented in section 5, 6 and 7, respectively. Our proposed parity preserving reversible D flip-flop, parity preserving reversible (7, 4) cyclic code encoder and decoder circuits are presented in section 8, 9 and 10, respectively. Comparison of the proposed circuits with the existing designs is also presented in section 11. Conclusions and references are in sections 12 and 13, respectively.

2. Basic Concepts

In this section brief background information about reversible and quantum logic gates and circuits, and also parity preserving reversible logic gates and circuits is presented.

2.1. Reversible and Quantum Gates, and Circuits

A gate, a circuit or a function is reversible if and only if there is a one-to-one mapping between its input and output. Therefore, a reversible gate has an equal number of inputs and outputs. Reversible logic gates can be implemented in various technologies such as CMOS circuits, optical circuits, and nanotechnology. Some parity preserving reversible gates are also implemented in QCA recently and are used for fault testing [19-22].

A 2*2 Feynman Gate [23], also known as controlled NOT (1-CNOT), is depicted in Fig. 1.a. It implements the logic functions: $P=A$, and $Q=A \oplus B$. That is, if the control input of CNOT is set to '0', then the gate acts as a BUFFER gate; otherwise, it acts as a NOT gate. The Feynman gate can be used as fan-out gate to copy a single bit. If the B input in Fig.1.a is set to '0' then two outputs of the Feynman gate are equal to the input A .

Toffoli [24] and Peres [25] gates are 3*3 reversible gates (Fig.1.b,c). Both of them are universal gates. That is, any logical reversible circuit can be implemented using each of these gates. The Feynman gate and the Peres gate (Fig.1.a,c) are one-through gates, i.e. one of the input lines is also output. The Toffoli gate (Fig.1.b) is two-through gate, i.e. two of the input lines are also outputs.

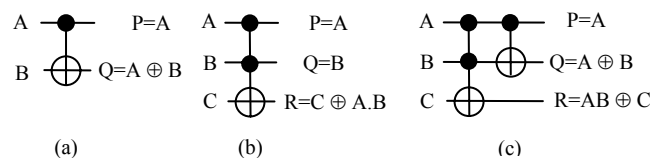


Fig.1 Reversible logic gates (a) Feynman gate (b) Toffoli gate (c) Peres gate

A 3*3 Toffoli gate has two control inputs that are copied to the first two outputs, and one other input that is complemented if all control inputs are 1s and is directly copied to the last output, otherwise.

Peres gate (PG), is equivalent to the transformation produced by a Toffoli gate followed by a Feynman gate [14].

A 4*4 reversible gate, HNFG [14] is depicted in Fig. 2. HNFG gate is 4-input, 4-output reversible gates. Furthermore, it is a two-through gate, which means that two input variables are also outputs.

Each HNFG gate can be used as two well-known 2*2 Feynman gates. It also can be used as “Copying Circuit” to increase fan-out because fan-out is not allowed in reversible circuits. It is suitable for a single copy of two bits with no garbage outputs [14]. As shown in Fig. 2, its quantum cost (QC) is only 2.

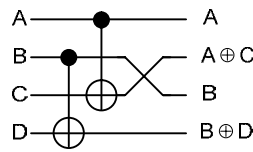


Fig.2. Reversible 4*4 HNFG gate

A 4*4 reversible gate, HCG [18] is depicted in Fig. 3. HCG gate is one-through gate which means that one of the input variables is also output. To the best of our knowledge, quantum realization of this gate is not proposed yet. Several other reversible gates are also proposed in some papers [13-14, 26-27].

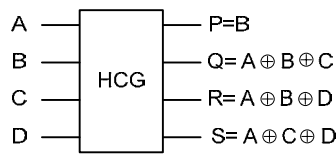


Fig.3 Reversible 4*4 HCG gate

A reversible circuit is usually depicted using a series of connected gates, similar to musical staves, on a number of parallel lines, similar to the musical lines. These lines are the inputs/outputs of the circuit. The gates are placed on these parallel lines. Using this notation, design of a reversible circuit is similar to composing a piece of music [9].

Quantum logic gates act on small units of data called quantum bits or simply qubits [3-4, 9-10]. Quantum logic gates are reversible and they can be represented by 2*2 unitary matrices. For example Feynman, Toffoli, Phase Shifter, V , V^\dagger and Hadamard gates are some quantum gates.

The V^\dagger gate is the Hermitian conjugate of V . The V and V^\dagger quantum gates have some properties that are shown in Eq. 1.

$$\begin{cases} V \times V = NOT \\ V \times V^\dagger = V^\dagger \times V = I \\ V^\dagger \times V^\dagger = NOT \end{cases} \quad (1)$$

This equation shows that two V or two V^\dagger gates in series are equivalent to a NOT gate. The equation also shows that a V and a V^\dagger in series, are equivalent to a BUFFER gate. The set of V , V^\dagger , and Feynman gates (TOFF2) is universal, i.e. any reversible or quantum logic gate can be realized using this set of gates [3-4, 9-10].

The *quantum cost* (QC) of a reversible logic circuit is defined as the number of 1×1 or 2×2 reversible or quantum logic gates which are needed to realize the gate or circuit because the quantum gates or circuits larger than 2×2 are not directly realizable in the quantum technology [3-4, 9-10].

2-2 Parity Preserving Reversible Gates and Circuits

Between reversible logic gates (circuits), those gates (circuits) which their input parity is the same as their output parity are called “parity preserving reversible gates (circuits)”. Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems [15-16]. Therefore it is important to construct parity preserving reversible gates and circuits. We have some problems using standard methods of error detection in reversible logic circuits, because fan-out is not allowed and it increases the number of gates. Garbage output is also one of the other main constraints in reversible logic design which we should take care of it.

There exist a few parity-preserving reversible gates. The Fredkin [28] gate (FRG) depicted in Fig. 4, the F2G [29] gate depicted in Fig.5, and the NFT gate depicted in Fig 6 are parity-preserving 3*3 reversible gates. These gates are parity preserving gates because their input parity $A \oplus B \oplus C$ is the same

as their output parity $P \oplus Q \oplus R$. The IG gate and the PPHCG gate are also parity preserving reversible gates. They are 4×4 parity preserving reversible gates and are depicted in Fig.7 and Fig.8 respectively. We propose their quantum realizations in this paper.

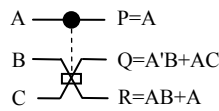


Fig.4 Parity Preserving Reversible Fredkin gate

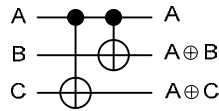


Fig.5 Parity Preserving Reversible F2G gate

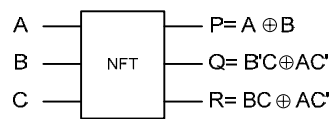


Fig.6 Parity-preserving reversible NFT gate

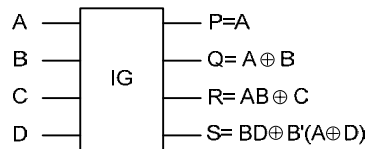


Fig.7 Parity-preserving reversible IG gate

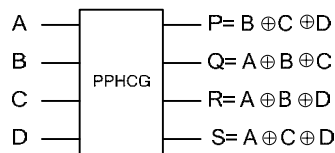


Fig.8 Parity-preserving reversible PPHCG gate

3. Our Proposed Quantum Realization of Parity Preserving Reversible IG Gate

A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [15-16]. In this case the input and output data can be checked in a manner that is off the computation's critical path. We need parity-preserving reversible gates in order to construct parity-preserving reversible circuits. Therefore in this section we propose a quantum equivalent circuit for parity preserving reversible IG gate. The proposed circuit is depicted in Fig. 9. The quantum cost of the proposed realization is only 7.

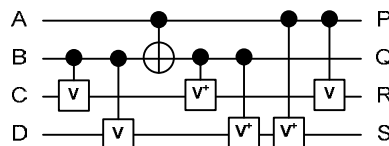


Fig.9 Our proposed equivalent quantum representation of parity preserving reversible IG gate. Its QC is only 7.

We can verify that the proposed circuit (Fig.9) is equivalent to the IG gate. The P output is equal to A. The Q output is equal to $A \oplus B$. The last two outputs (R and S) can not directly be expressed in term of

inputs, because of the existence of quantum V and V+ gates. To verify the R and S outputs, we can write their truth tables. For example if ABCD inputs are 1101, from left to right, the status of the V and V+ gates on C to R path, and D to S path, are as follows:

For C to R path (Left to Right):

- 1- V gate in C to R path is active because its control (B) is '1'.
- 2- V+ gate in C to R path is inactive because its control (B⊕A) is '0'.
- 3- V gate in C to R path is active because its control (A) is '1'.

Thus, in the C to R path there is a $V*V=NOT$ operation that results to $R = '1'$. From the annotation of R we also obtain $R = AB⊕C=1 ⊕ 0 = 1$.

For D to S path (Left to Right):

- 1- V gate in D to S path is active because its control (B) is '1'.
- 2- V+ gate in D to S path is inactive because its control (B⊕A) is '0'.
- 3- V+ gate in D to S path is active because its control (A) is '1'.

Therefore, in the D to S path there is a $V*V+=I$ operation that results to $S = '1'$. From the annotation of S we also obtain $S = BD⊕B'.(A⊕D) = 1⊕ 0.(1⊕1) = 1 ⊕ 0 = 1$.

Other 15 states can be checked in the same manner.

4. Our Proposed Quantum Realization of Parity Preserving Reversible PPHCG Gate

As we stated in section 3, we need parity-preserving reversible gates in order to construct parity-preserving reversible circuits. Therefore in this section we also propose a quantum equivalent circuit for another parity preserving reversible gate, named PPHCG. The proposed circuit is depicted in Fig. 10. The quantum cost of the proposed realization is only 6.

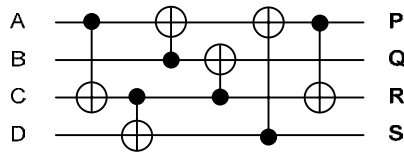


Fig.10 Our proposed equivalent quantum representation of parity preserving reversible PPHCG gate. Its QC is only 6.

We can verify that the proposed circuit (Fig.10) is equivalent to the PPHCG gate. The P output is equal to $B⊕C⊕D$. The Q output is equal to $A⊕B⊕C$. The R output is equal to $A⊕B⊕D$, and The S output is equal to $A⊕C⊕D$.

5. Our Proposed Reversible Hamming Code Generator

Hamming Code is a reliability concept that is founded by Richard Hamming. It can *correct* any single error and also can *detect* any double errors (two separate errors). Now, this code is one of the most commonly used codes to perform Single Error Correction - Double Error Detection (SEC-DED) [18]. Hamming Code uses extra bits in order to correct a single error, or to detect double errors. Imagine a message having four data bits (D3-D0) and three extra error checking bits. Therefore a 7-bit codeword is to be transmitted. This would be called a (7, 4) code. The three bits to be added are three even parity bits (P), where the parity bit is computed on different subsets of the message bits using Eq.2 [18]:

$$\begin{aligned} P1 &= D0⊕D1⊕D3 \\ P2 &= D0⊕D2⊕D3 \\ P3 &= D1⊕D2⊕D3 \end{aligned} \quad (2)$$

A (7, 4) bit reversible Hamming code generator is proposed and depicted in Fig 11. It is shown that its quantum cost is only 8. The proposed design requires three constant inputs. It generates the 7-bit hamming code (H7 to H1) without any garbage outputs.

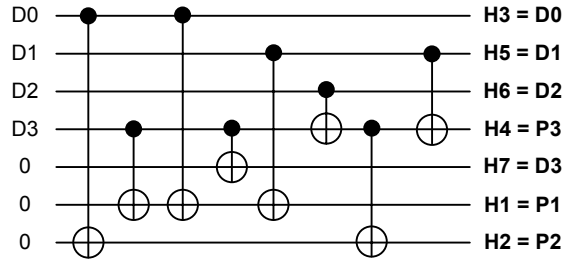


Fig.11 Quantum realization of our proposed reversible (7,4) Hamming code generator. Its QC is only 8.

6. Our Proposed Parity Preserving Reversible Hamming Code Generator

First we define the minimum number of input and output of a parity preserving reversible Hamming code generator. We also define the minimum number of constant input and minimum number of garbage output of a parity preserving reversible Hamming code generator.

Theorem 1: Parity preserving reversible Hamming code generator requires at least 8 inputs and 8 outputs. It produces at least 1 garbage output and it needs a minimum of 4 constant inputs.

Proof: We have 4 main inputs and 7 main outputs. Since the circuit is fault tolerant, the input parity should be equal to the output parity. Thus we need at least one output line (garbage output) to make them equal. As a result the number of output lines is at least 8 because we have 7 main outputs plus 1 garbage output. Therefore we also need 8 input lines. Thus 4 constant inputs should be added to the main input lines.

Figure 12 shows the implementation of our proposed parity preserving reversible (7,4) bit Hamming code generator. It is shown that the quantum cost of the proposed circuit is only 10. The proposed circuit requires four constant inputs and generates a single garbage output. Thus the proposed circuit is optimum in terms of number of constant inputs and number of garbage outputs (theorem 1). The circuit is better than the existing counterparts in term of quantum cost, number of constant inputs, number of garbage outputs and size of the circuit.

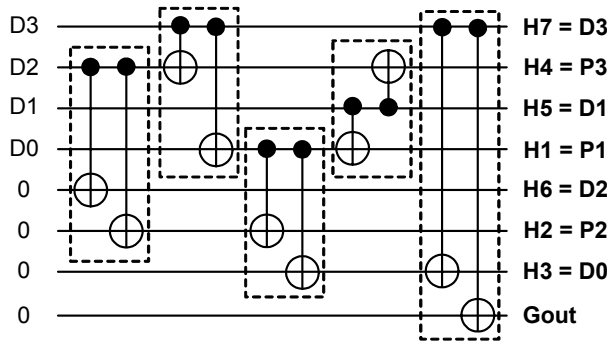


Fig.12 Quantum realization of our proposed parity preserving reversible (7,4) Hamming Code generator. Its QC is only 10.

7. Our Proposed Parity Preserving Reversible Hamming Code Error Detector

The Hamming code uses extra redundant bits to check for errors, and performs the checks with special check equations. Check bits are computed on different subsets of the Hamming code bits using below mentioned equations [18]:

$$\begin{aligned}
 C1 &= H1 \oplus H3 \oplus H5 \oplus H7 \\
 C2 &= H2 \oplus H3 \oplus H6 \oplus H7 \\
 C3 &= H4 \oplus H5 \oplus H6 \oplus H7
 \end{aligned}
 \tag{3}$$

If all the three check bits are zero then we have no error, otherwise it indicates the position bit of error.

Theorem 2: Parity preserving reversible Hamming code error detector requires at least 4 garbage outputs. It can be implemented in such a way that it does not need any constant input.

Proof: We have 7 main inputs and 3 main outputs. Thus we have at least 4 garbage outputs. Since the circuit is fault tolerant, the input parity should be equal to the output parity. It is possible to make them equal using the garbage bit functions. There is no need to add any constant input.

The proposed parity preserving reversible Hamming code error detector circuit is shown in Fig. 13. The circuit has parity preserving property. Therefore it is capable of detecting fault in the circuit. It is shown that the quantum cost of the proposed circuit is only 10. The proposed circuit does not need any constant input. It also generates four garbage output. Thus the circuit is optimum in terms of number of garbage outputs and number of constant inputs (theorem 2). The circuit is better than the existing counterparts in term of number of constant inputs, number of garbage outputs and size of the circuit.

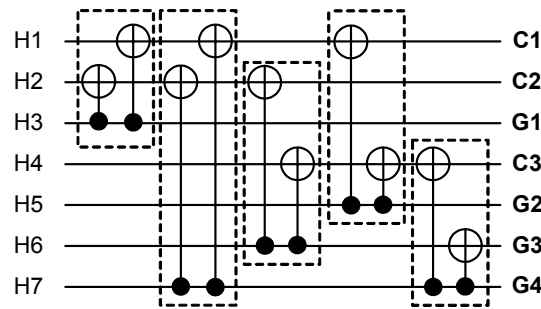


Fig.13 Quantum realization of our proposed parity preserving reversible (7,4) Hamming code error detector. Its QC is only 10.

8. Our Proposed Parity Preserving Reversible D Flip-Flop

In this section a new parity preserving reversible D latch and its corresponding D Flip-Flop using master slave strategy [31-35] is presented. The proposed circuits are depicted in Fig. 14. The parity preserving D Flip Flop requires two block of D latch and a F2G gate. Each D latch needs a Fredkin gate and an F2G gate. Thus the proposed parity preserving D Flip Flop requires three F2G and two Fredkin gates and its QC is 16. We use this circuit later in the design of new parity preserving reversible (7, 4) cyclic code encoder/decoder circuits.

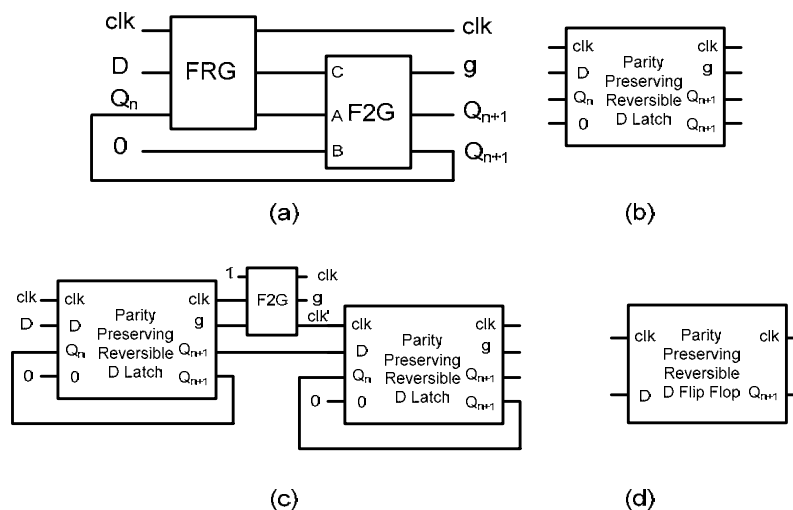


Fig.14 our proposed parity preserving reversible clocked D Latch and corresponding D Flip-Flop (a) D Latch structure; (b) D Latch block diagram; (c) D Flip Flop structure; (d) D Flip Flop block diagram.

9. Our Proposed Parity Preserving Reversible (7,4) Cyclic Code Encoder

Cyclic codes can be used in applications where burst errors occur and a group of adjacent bits is affected [30]. In this section a new parity preserving reversible (7, 4) cyclic code with the generator polynomial $g(x)=1+x+x^3$ is presented.

In a cyclic code, the polynomial representing the data is multiplied by a generator polynomial, $g(x)$, in order to encode the data and to generate the codeword [30]. For 4 bit input data, the produced code words with the generator polynomial, $g(x)=1+x+x^3$, are defined in table 1. Since degree of $g(x)$ is 3, 3-bit burst errors can be detected by this code [30]. Our proposed parity preserving reversible (7, 4) cyclic code encoder with the generator polynomial $g(x)=1+x+x^3$ is depicted in Fig. 15. Its QC is 8. The code words are as follows:

$$\begin{aligned} C_0 &= d_0 \\ C_1 &= d_0 \oplus d_1 \\ C_2 &= d_2 \oplus d_1 \\ C_3 &= d_2 \oplus d_3 \oplus d_0 \\ C_4 &= d_3 \oplus d_1 \\ C_5 &= d_2 \\ C_6 &= d_3 \end{aligned}$$

Table 1. Input data and codeword for (7, 4) cyclic code with the generator polynomial $g(x)=1+x+x^3$.

d_0	d_1	d_2	d_3	c_0	c_1	c_2	c_3	c_4	c_5	c_6
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1	0	1
0	0	1	0	0	0	1	1	0	1	0
0	0	1	1	0	0	1	0	1	1	1
0	1	0	0	0	1	1	0	1	0	0
0	1	0	1	0	1	1	1	0	0	1
0	1	1	0	0	1	0	1	1	1	0
0	1	1	1	0	1	0	0	0	1	1
1	0	0	0	1	1	0	1	0	0	0
1	0	0	1	1	1	0	0	1	0	1
1	0	1	0	1	1	1	0	0	1	0
1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0	1
1	1	1	0	1	0	0	0	1	1	0
1	1	1	1	1	0	0	1	0	1	1

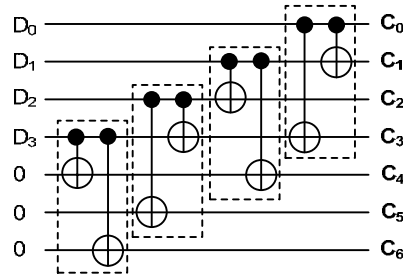


Fig. 15. Our proposed parity preserving reversible (7, 4) cyclic code encoder circuit with the generator polynomial $g(x)=1+x+x^3$

10. Our Proposed Parity Preserving Reversible (7, 4) Cyclic Code Decoder

We need parity preserving reversible D flip-flops in the structure of the parity preserving reversible (7, 4) cyclic code decoder. Thus we use the parity preserving reversible D flip-flop which is proposed in section 8 (Fig. 14). If we suppose that C is a binary cyclic code with the generator polynomial $g(x)=1+x+x^3$ then its check polynomial would be $h(x)=1+x+x^2+x^4$, and the corresponding parity check matrix is [30]:

$$H = \begin{bmatrix} 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix} \quad (2)$$

Our proposed parity preserving reversible (7, 4) cyclic code decoder with the generator polynomial $g(x)=1+x+x^3$ is depicted in Fig. 16. It needs two parity preserving reversible Feynmann Double Gate (F2G), and three parity preserving reversible D flip-flops. In this structure, after 4th clock cycle, if the registers values are [000], then C(x) is a codeword and the output d(x) is a valid data; but if the registers values matches one column of the columns of the parity check matrix H, then it determines that a single bit error has occurred in the corresponding position of the matching column in matrix H. in this condition the error can be corrected. If the registers values after 4th clock cycle are not zero, and are not equal to any of the columns of matrix H, then it determines that a multiple bit error has occurred. Thus the circuit can detect multiple bit errors, and it can correct single bit error.

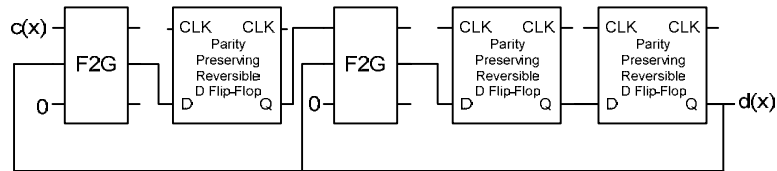


Fig. 16. Our proposed parity preserving reversible (7, 4) cyclic code decoder circuit with the generator polynomial $g(x)=1+x+x^3$

11. Comparison

In this paper we presented quantum equivalent representation of parity preserving IG gate. QC of the proposed circuit is 7. We also presented quantum equivalent representation of parity preserving PPHCG gate. QC of the proposed circuit is only 6. A parity preserving reversible D flip-flop is also proposed. Its QC is 16. Two new (7, 4) reversible Hamming code generator circuits are also proposed. One of them is parity preserve. The proposed parity preserving reversible circuit is compared with the previous designs. To compare these designs, the quantum cost (QC), number of constant inputs, number of garbage outputs and size of the circuit are considered. Table 2 compares the proposed parity preserving reversible circuit with the existing counterparts.

We also proposed a new parity preserving (7,4) reversible Hamming code error detector circuit. The design is better than the existing designs in term of number of constant inputs, number of garbage outputs and size of the circuit. Table 3 compares the proposed parity preserving reversible circuit with the existing counterparts. It is to be noted that only one of the existing designs in table 3 is parity preserving reversible circuit. Another one is not parity preserving. Our design is also parity preserving reversible circuit. From table 2 and 3 we can conclude that our designs are better than the existing designs. The proposed circuits are optimum in terms of number of constant inputs and number of garbage outputs.

Parity preserving reversible (7, 4) cyclic code encoder/decoder circuits with the generator polynomial $g(x)=1+x+x^3$ are also studied. In the best of our knowledge parity preserving reversible (7, 4) cyclic code encoder/decoder circuits are not proposed in the past literatures.

Table 2: Specifications of parity preserving reversible Hamming code generator circuit designs proposed in this and other papers.

Design	Gate Types	No. of Garbage Outputs	Quantum Cost	No. of Constant Inputs	Size
James [18]	F2G, PPHCG	5	14	8	12*12
James [18]	F2G	4	12	7	11*11
New	F2G	1*	10	4*	8*8
Improvement	-	80%-75%	28.57%-16.66%	50%-42.85%	33.3%-27.27%

* Optimum values

Table 3: Specifications of reversible Hamming code error detector circuit designs proposed in this and other papers

Design	Parity Preserving Property	Gate Types	No. of Garbage Outputs	Quantum Cost	No. of Constant Inputs	Size
James [18]	No	HCG, FG	4	Not Known	0	7*7
James [18]	Yes	F2G	6	10	2	9*9
New	Yes	F2G	4*	10	0*	7*7
Improvement	-	-	0%-33.33%	-	0%-100%	0%-22.22%

* Optimum values

12. Conclusions

Quantum equivalent representations of parity preserving IG gate and PPHCG gate are proposed. The quantum costs of these gates are 7 and 6, respectively. PPHCG gate is used in some of the previous designs of parity preserving reversible Hamming Code generator, which are compared with our new designs. Therefore it is important to have PPHCG quantum realization for a fair comparison of the existing designs with our new designs. A parity preserving reversible D flip-flop is also proposed. Its QC is 16.

Two new reversible Hamming code generator circuits are also proposed. One of them is parity preserve. The proposed parity preserving reversible circuit is compared with the previous designs. A new parity preserving (7, 4) reversible Hamming code error detector circuit is also presented. The designs are better than the existing designs in term of quantum cost, size of the circuit, number of constant inputs and number of garbage outputs. Parity preserving reversible (7, 4) cyclic code encoder/decoder circuits with the generator polynomial $g(x)=1+x+x^3$ are also studied for the first time.

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